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Methods of Measurement for Semiconductor Materials, Process Control, and Devices

Quarterly Report

April 1 to June 30, 1973

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Methods of Measurement for Semiconductor Materials, Process Control, and Devices

Quarterly Report, April 1 to June 30, 1973

W. Murray Bullis, Editor

Electronic Technology Division
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FOREWORD

The Joint Program on Methods of Measurement for Semiconductor Materials, Process Control, and Devices was undertaken in 1968 to focus NBS efforts to enhance the performance, interchangeability, and reliability of discrete semiconductor devices and integrated circuits through improvements in methods of measurement for use in specifying materials and devices and in control of device fabrication processes. These improvements are intended to lead to a set of measurement methods which have been carefully evaluated for technical adequacy, which are acceptable to both users and suppliers, which can provide a common basis for the purchase specifications of government agencies, and which will lead to greater economy in government procurement. In addition, such methods will provide a basis for controlled improvements in essential device characteristics, such as uniformity of response to radiation effects.

The Program is supported by the National Bureau of Standards,* the Defense Nuclear Agency,† the Defense Advanced Research Projects Agency,× the U.S. Navy Strategic Systems Project Office,§ the Air Force Weapons Laboratory,+ and the Atomic Energy Commission.¶ Although there is not a one-to-one correspondence between the tasks described in this report and the cost centers through which the Program is supported, the concern of certain sponsors with specific parts of the Program is reflected in planning and conduct of the work.

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METHODS OF MEASUREMENT FOR SEMICONDUCTOR MATERIALS, PROCESS CONTROL, AND DEVICES

QUARTERLY REPORT
APRIL 1 TO JUNE 30, 1973

This quarterly progress report, twentieth of a series, describes NBS activities directed toward the development of methods of measurement for semiconductor materials, process control, and devices. Significant accomplishments during this reporting period include (1) completion of an initial identification of the more important problems in process control for integrated circuit fabrication and assembly as a basis for an expanded effort to be conducted in cooperation with ARPA, (2) completion of preparations for making silicon bulk resistivity wafer standards available to the industry, and (3) undertaking of new work to establish the relationship between carrier mobility and impurity density in silicon and to investigate test patterns for use in process control and evaluation. Because of the general applicability of the first of these, a summary of the findings is presented in a separate appendix. Work is continuing on measurement of resistivity of semiconductor crystals; characterization of generation-recombination-trapping centers, including gold, in silicon; evaluation of wire bonds and die attachment; study of scanning electron microscopy for wafer inspection and test; measurement of thermal properties of semiconductor devices; determination of S-parameters and delay time in junction devices; and characterization of noise and conversion loss of microwave detector diodes. Supplementary data concerning staff, standards committee activities, technical services, and publications are also included as appendices. This is the last report in this form; future reports in this series will appear under the title, Semiconductor Measurement Technology.

Key Words: Beam leads; carrier lifetime; delay time; die attachment; electrical properties; electronics; epitaxial silicon; generation centers; gold-doped silicon; methods of measurement; microelectronics; microwave diodes; mobility; pull test; recombination centers; resistivity; resistivity standards; scanning electron microscopy; semiconductor devices; semiconductor materials; semiconductor process control; silicon; S-parameters; spreading resistance; thermal resistance; thermally stimulated properties; trapping centers; wire bonds.

1. INTRODUCTION

This is the twentieth quarterly report to the sponsors of the Joint Program on Methods of Measurement for Semiconductor Materials, Process Control, and Devices. It summarizes work on a wide variety of measurement methods that are being studied at the National Bureau of Standards. The Program is a continuing one, and the results and conclusions reported here are subject to modification and refinement.

The work of the Program is divided into a number of tasks, each directed toward the study of a particular material or device property or measurement technique. This report is subdivided according to these tasks. Highlights of activity during the quarter are given in section 2. Section 3 deals with tasks on methods of measurement for materials; section 4, with those on methods of measurement for process control; and section 5, with those on methods of measurement for devices. References for each section are listed in a separate subsection at the end of that section.

The report of each task includes the long-term objective, a narrative description of progress made during this reporting period, and a listing of plans for the immediate future. Additional information concerning the material reported may be obtained directly from individual staff members identified with the task in the report. The organization of the Joint Program staff and telephone numbers are listed in Appendix A.

An important part of the work that frequently goes beyond the task structure is participation in the activities of various technical standardizing committees. The list of personnel involved with this work given in Appendix B suggests the extent of this participation. Additional details of current standardization activities not associated with a particular task are given in section 2.

Background material on the Program and individual tasks may be found in earlier reports in this series as listed in Appendix D. From time to time, publications are prepared that describe some aspect of the program in greater detail. Current publications of this type are also listed in Appendix D. Reprints or copies of such publications are usually available on request to the author.

2. HIGHLIGHTS

Significant accomplishments during this reporting period include (1) completion of an initial identification of the more important problems in process control for integrated circuit fabrication and assembly as a basis for an expanded effort to be conducted in cooperation with ARPA, (2) completion of preparations for making silicon bulk resistivity wafer standards available to the industry, and (3) undertaking of new work to establish the relationship between carrier mobility and impurity density in silicon and to investigate test patterns for use in process control and evaluation.

Highlights of these and other ongoing activities are presented in this section; details of progress in technical areas are given in subsequent sections of the report. This section includes a summary of standardization activities being carried out by program staff members and concludes with a brief description of a program expansion to be undertaken during the next quarter.

Some rearrangement of task areas was made during the quarter in recognition of changing priorities. The results of work on carrier mobility and test pattern evaluation are reported in separate sections. Work on gold-doped silicon was consolidated with that on generation-recombination-trapping centers. No work was done this quarter on study of infrared methods; this section, omitted in this report, will reappear when work is resumed. The section entitled Wire Bond Evaluation has been renamed Interconnection Bond Evaluation.

Resistivity — Silicon bulk resistivity standard sets are now available to the industry. Procedures for obtaining sets are detailed in the official announcement, reproduced as Appendix E. These wafer standards, to be used with four-probe resistivity test sets, have a conservatively stated precision of ±2.5 percent of their measured value.

An initial calibration curve for the spreading resistance for p-type silicon as a function of resistivity was generated. Definite irregularities in spreading resistance as a function of resistivity were noted in the region above 1 Ω·cm. The corresponding calibration curve for n-type silicon wafers is now being generated.

A theoretical study was made to examine the region over which the junction capacitance-voltage method is useful in profiling the heavily doped side of a p^+n or n^+p junction. The sensitivity of the diffused layer profile to the estimate of background doping density was explored, and it was concluded that a meaningful profile can be obtained for the diffused layer at densities up to 30 times the background doping density.

Generation-Recombination-Trapping Centers — A simplified apparatus for measuring the thermally stimulated properties of a p-n junction was constructed and

tested. It has both a fast thermal cycle time and a rapid specimen throughput, and it is inexpensive. The thermally stimulated current of a gold-doped p^+n junction was found to display a distinct peak, confirming earlier theoretical predictions.

Simplified expressions for finding the carrier lifetime in diodes with various base width from reverse recovery measurements were evaluated and shown to be applicable in the transition region where the base width is about equal to the diffusion length. Surface photovoltage lifetime measurements were successfully made on an epitaxial n/p wafer with n^+ pockets diffused at the n/p interface by limiting the measurements to wavelengths which do not penetrate into the p-substrate.

Computer print-out tables of resistivity of gold-doped silicon as a function of gold density were prepared. These tables were derived from theoretical equations presented previously.

Carrier Mobility — This task area was initiated to assist in resolution of difficulties encountered in relating carrier mobility in silicon to impurity density and in calculation of carrier mobility in regions of mixed scattering. The effort will be coordinated with activities of the Mobility Section of ASTM Committee F-1 on Electronics. The initial step was to summarize the existing situation by comparing theoretical calculations of mobility with empirical relationships based on existing experimental data. Not only do the theoretical curves deviate from the experimental results in regions of mixed scattering, but there are discrepancies in the experimental results, particularly for p-type silicon in the range of impurity density from 10^{16} to 10^{19} cm^{-3}.

Die Attachment Evaluation — Computations using the TRUMP thermal analysis program were carried out using boundary conditions appropriate to (1) a round silicon chip on an infinite heat sink and (2) a simplified mesa-diode-and-header structure. Good agreement was achieved in the first case, not in the second.

The results of long-term, single-operator measurements of thermal response on transistor chips mounted with and without voids suggest that devices with voids can be detected by measurements of the response of the temperature sensitive parameter, emitter-base voltage, to a heating pulse with the device mounted in an ordinary socket without special heat sinking.

Interconnection Bond Evaluation — The resolution-of-forces equations were used to calculate the effects on the measured pull strength of ultrasonic wedge bonds which occur when the pull test parameters are varied over a range of values similar to that which might be obtained in industrial use. The results for a typical example indicate that the pull angle ϕ must be controlled to within 10 deg if the reproducibility of the test is to be better than 30 percent, but other parameters need not be so well controlled.

Feasibility studies have shown that aluminum ribbon wire can be ultrasonically bonded to copper thick film substrates. The vibration modes of two long bonding tools were studied during bonding. A study of beam-lead bonding tests was begun. A phase-locked-loop ultrasonic bonding power supply was characterized and certain instabilities identified. Pull test specifications were prepared for large diameter aluminum wire. Studies of the bonding characteristics of fine gold wire were initiated.

Scanning Electron Microscopy — Additional accessories were installed on the scanning electron microscope, preliminary studies were made using the voltage contrast mode of operation, and the literature search for data on device degradation from inspection by the scanning electron microscope continued.

Test Pattern Evaluation — The results of the first fabrication run on test pattern NBS-2 identified several problem areas in the in-house bipolar process. The boron nitride base diffusion was studied using the base sheet resistor test structure. Variations of resistivity over the entire slice as low as ±3.2 percent (two relative sample standard deviations) were observed.

Thermal Properties of Devices — A summary of the results of the preliminary round-robin experiment on thermal resistance being conducted in cooperation with EIA-JEDEC Committee JC-25 on Power Transistors confirmed the previously reported results that the V_{CB} technique gives lower values of thermal resistance then the V_{BE} base-and-collector switching technique and that the latter gives lower values then the V_{EB} emitter-only switching technique.

A study was undertaken to determine whether the measurement of d-c current gain, h_{FE}, as a function of collector-emitter voltage, V_{CE}, for constant collector current and case temperature can be used as a screen to predict accurately when the electrical measurement of thermal resistance deviates significantly from the thermal resistance as derived from the measurement of peak junction temperature. It had been observed previously that in cases where the change in h_{FE} is abrupt, the deviation occurs at a value of V_{CE} very close to that at which h_{FE} changes abruptly. In cases of less abrupt changes in h_{FE}, it was found that significant deviations may occur at voltages below that which h_{FE} is a maximum; hence, the h_{FE} screen may not be an accurate predictor.

Microwave Device Measurements — The mixer conversion loss repeatability studies were continued using a Schottky-barrier diode. This diode was found to be sensitive to mechanical shock, as were the point-contact types used previously. In the standards area, a limited revision was made of the IEC standard on microwave mixer measurements, and mixer terminology that appears to be acceptable to both the IEEE and the EIA was prepared in collaboration with members of the latter.

Carrier Transport in Junction Devices — Measurements were made with the Sandia bridge on a 2N2907A silicon *p-n-p* transistor after gain degradation by neutron irradiation. The results showed that the large variations in delay time then measured could be reduced significantly by applying the appropriate correction factor. However, unlike the case of a 2N2219 *n-p-n* silicon transistor previously reported, a significant increase in delay time was observed.

In the S-parameter round robin, the between-laboratory variability for transistor measurements was compared with the between-laboratory variability of the measurements on the R-C networks made under the same conditions and found to be within the expected range, indicating that there is no basis for concluding that additional variability is introduced in the transistor measurements.

Standardization Activities — Standardization activities directly related to particular task areas are reported with the appropriate tasks. However, many of the standardization activities undertaken by program staff are broader than the technical tasks described in the following sections. These activities, which are reported here, involve general staff support in committees, coordination of efforts which may encompass a variety of tasks, and participation in areas where no direct in-house technical effort is underway.

Sixteen staff members participated in meetings of ASTM Committee F-1 on Electronics, held in Gaithersburg on June 12-14. In preparation for this meeting 10 documents were edited at the subcommittee or committee level.

Staff members also attended meetings of EIA-JEDEC Committees JC-25 on Power Transistors and JC-22 on Rectifier Diodes and Thyristors and of the IEEE Electron Devices Group Standards Committee.

Program Expansion — Beginning next quarter, the scope of the program will be expanded significantly with the inclusion of a new effort on Advancement of Reliability, Processing, and Automation for Integrated Circuits with the National Bureau of Standards (ARPA/IC/NBS), sponsored by the Defense Advanced Research Projects Agency (ARPA).

This new effort, which addresses critical Defense Department problems in the yield and reliability of integrated circuits, responds to a need for improved measurement methods and associated technology for controlling and automating key processing and assembly procedures and is being developed in concert with the reliability laboratories of the three services. Its major thrusts are the development of well-documented test procedures and measurement technology for use on semiconductor device production lines and the dissemination of such information to the electronics community. Application of the output by industry is expected to contribute to higher yields,

lower cost, higher reliability, and greater availability of special devices needed by the Department of Defense.

To assist in the selection of activities to be undertaken in this effort, initial consultations were completed with representatives of the electronics community to identify the more important measurement problems in process control for silicon wafer fabrication and device assembly, primarily of bipolar and MOS digital integrated circuits. A widely expressed general need was for more nondestructive, direct, and rapid production-type measurement methods. Specific critical measurement needs were identified in the following areas: (1) the starting silicon material in regard to defects and resistivity; (2) silicon diffused and epitaxial layers in regard to thickness, doping profiles, and sheet resistivity; (3) oxide films in regard to stability and impurities; (4) photolithographic procedures in regard to mask inspection, photoresist materials and their use, and pin holes; and (5) hermeticity. Problems were also identified in connection with the control of incoming materials, ion implantation processes, and surface cleanliness. Additional details are given in Appendix F.

This program is to be announced at a Workshop on Measurement Needs for Controlling IC Processing and Assembly Procedures on September 7, 1973 in Palo Alto, California. The workshop will have the dual objective of formally announcing the program to the semiconductor industry and providing the industry with a forum for providing additional input related to process control measurement requirements. The workshop will be held concurrently with the final day of the fall meeting of ASTM Committee F-1 on Electronics.

This workshop, first of a series, will focus on nonproprietary measurement problems in which semiconductor device manufacturers, their suppliers, and their customers share a concern. The morning session will feature presentations on the ARPA/IC/NBS Program; earlier activities of NBS in electronic measurement technology; and some conclusions drawn from discussions with industrial representatives regarding needed process control improvements. In the afternoon small groups will be formed to discuss specific process control problems and measurement needs related to silicon, oxides, photolithography, and assembly, as well as dissemination problems. The discussions will be summarized at the end of the workshop.

In anticipation of the expanded effort, new project areas to deal with hermeticity, photolithography, and oxide characterization will be established early next quarter.

This report is the last to appear under the title, Methods of Measurement for Semiconductor Materials, Process Control and Devices. The series will continue under the title, Semiconductor Measurement Technology. Its distribution and availability will not be affected by the change in title.

3. SEMICONDUCTOR MATERIALS

3.1. RESISTIVITY

Objective: To develop methods suitable for use throughout the electronics industry for measuring resistivity of bulk, epitaxial, and diffused silicon wafers.

Progress: Silicon bulk resistivity standard sets are now available to the industry. Procedures for obtaining sets are detailed in the official announcement, reproduced as Appendix E. These wafer standards, to be used with four-probe resistivity test sets, have a conservatively stated precision of ±2.5 percent of their measured value.

An initial calibration curve for the spreading resistance for p-type silicon as a function of resistivity was generated. Definite irregularities in spreading resistance as a function of resistivity were noted in the region above 1 Ω·cm. The corresponding calibration curve for n-type silicon wafers is now being generated.

A theoretical study was made to examine the region over which the junction capacitance-voltage method is useful in profiling the heavily doped side of a p^+n or n^+p junction. The sensitivity of the diffused layer profile to the estimate of background doping density was explored, and it was concluded that a meaningful profile can be obtained for the diffused layer at densities up to 30 times the background doping density.

Silicon Resistivity Standards — Sets of bulk silicon wafers consisting of one each nominal 0.1 Ω·cm and 10 Ω·cm boron-doped modified float-zoned wafers were prepared and their resistivity was individually measured according to ASTM Method F-84 [1]. Tests were conducted to disclose systematic biases due to the instrument, the operator, or measurement at a position accidentally slightly away from the center of the wafer. The results indicate that the calibrated resistivity values are safely within the stated certified tolerance of ±2.5 percent. The ultimate value of precision attainable on such standard resistivity wafers is to be determined during the next 12 to 18 months by a carefully controlled experiment between NBS and industrial laboratories selected by NBS based on past experience in resistivity round-robin tests. However, all other groups acquiring standard resistivity wafer sets are also invited to submit data taken on their wafers in order to give a greater overall perspective of the durability of such resistivity standards in a wide variety of measurement environments. (J. R. Ehrstein, M. Cosman, F. H. Brewer, and D. R. Ricks)

Other Standards Activities — The analysis of the results of the round-robin test on measuring the sheet resistance of epitaxial silicon layers according to ASTM Method F-374 [2] was completed. The results of this round robin, conducted in

Table 1 — Summary of Results of Epitaxial Sheet Resistance Round Robin

Specimen		1	1A	2	3	3A	4	5	6
Layer type		*p*	*p*	*p*	*p*	*p*	*n*	*n*	*n*
Substrate type		*n*	*n*	*n*	*n*	*n*	*p*	*p*	*p*
Nominal sheet resistance, Ω		15000	10840	600	390	1390	1100	1880	4600
Nominal layer thickness, μm		10.7	12.5	13.2	2.3	3.3	12.1	7.8	16.8
Criterion 1	No. of labs	1	6	8	4	5	10	10	10
	Multi-lab relative sample std. dev., %	NA	140	3.6	16	19	2.7	1.5	1.9
	Average single-lab relative sample std. dev., %	0.44	8.5	1.0	5.6	1.4	0.35	0.22	0.42
Criterion 2	No. of labs	3	6	12	6	7	13	12	13
	Multi-lab relative sample std. dev., %	0.60	3.8	4.1	14	3.5	2.4	1.4	1.8
	Average single-lab relative sample std. dev., %	1.5	1.6	1.5	6.9	1.1	0.37	0.22	0.47
Criteria 1&2	No. of labs	1	5	8	3	5	10	10	10
	Multi-lab relative sample std. dev., %	NA	3.2	3.6	10.5	3.8	2.7	1.5	1.9
	Average single-lab relative sample std. dev., %	0.44	1.6	1.0	2.7	0.90	0.35	0.20	0.40

conjunction with ASTM Committee F-1 on Electronics, are listed in table 1. After data from one laboratory were dropped completely for failure to follow the required measurement procedure, two criteria were established for the rejection of erroneous data. First, data were rejected from laboratories which failed to meet the requirements on measurement of analog test circuits as specified in the method of test [2]. Second, data were analysed for the presence of outliers [3], which were then rejected. Although five of the specimens showed various degrees of fracture before the test was completed, not all corresponding data appeared as outliers. If both criteria were applied, the multilaboratory precision was 12 percent or less (three relative sample standard deviations) for six of the eight specimens measured.

(J. R. Ehrstein and F. H. Brewer)

Spreading Resistance Methods — Preparatory to the use of the spreading resistance method to study semiconductor device structures and to study the effect of variation in measurement conditions, such as probe material, probe load, rate of

probe descent, and nature of semiconductor surface, on the measurement itself, it was necessary to generate an empirical calibration curve to relate bulk resistivity as measured by the four-probe method [1] with the measured spreading resistance of a given silicon wafer. A calibration curve was constructed for *p*-type specimens; another is being constructed for *n*-type specimens. Some fifty *p*-type specimens covering the room-temperature resistivity range 0.001 to 100 Ω·cm were selected from available material. Slices were cut and prepared with one chem-mechanically polished surface [4] which has been found to give reasonably stable measurement conditions and one lapped surface. Four-probe measurements were made on the lapped surface of each slice to characterize its radial resistivity uniformity. Spreading resistance measurements were made over a 2- to 3-mm long center section of the chem-mechanically polished side of each slice. The mean value of spreading resistance for each slice was plotted against its resistivity as measured at the center of the slice. Although the linear regression of the data points appears to be a highly accurate representation over most of the range, above 1 Ω·cm differences in measured spreading resistance up to 80 percent were encountered in cases where two or more specimens had nearly the same resistivity. These differences were substantially greater than the gross radial resistivity variations measured by the four-probe method. Periodic tests of a *p*-type reference wafer during the course of this calibration procedure showed that changes in the operating characteristics of the spreading resistance probes did not result in variations of spreading resistance greater than 10 percent. An explanation for this disparity is being sought.

In order to study the depth profile of device structures it is necessary to have a process for polishing the specimen of interest at a very shallow angle to open the various device layers to the spreading resistance probes. Several polishing methods were tried to obtain an angle-polished surface which is free of visible scratches and other damage and a well defined vertex of the angle between the original top surface of the structure and the newly opened angle-polished surface. Of the methods investigated, which included very fine diamond grit polishing and chem-mechanical polishing, both by hand and by machine, against several backing materials, a surface polished chem-mechanically in an oscillating tub polisher against a backing plate of methyl methacrylate appears to be essentially damage-free and to have a well defined vertex. However, if the width of the section to be angle polished exceeds 4 or 5 mm, curvature was noticed at the interface between the top surface and the angle-polished surface. The effect of static load on quality of the polished surface has not yet been studied. (J. R. Ehrstein)

Capacitance-Voltage Methods — A theoretical investigation was made into the feasibility of using junction capacitance-voltage (C-V) measurements for profiling

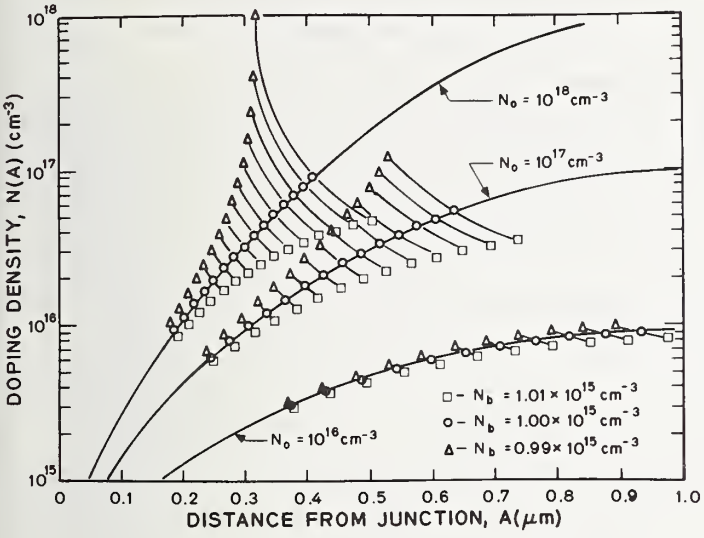
DOPING DENSITY, N(A) (cm⁻³)
DISTANCE FROM JUNCTION, A(μm)
N₀ = 10¹⁸cm⁻³
N₀ = 10¹⁷cm⁻³
N₀ = 10¹⁶cm⁻³
□ - N_b = 1.01 × 10¹⁵ cm⁻³
○ - N_b = 1.00 × 10¹⁵ cm⁻³
△ - N_b = 0.99 × 10¹⁵ cm⁻³

Figure 1. Doping profiles obtained from junction C-V measurements for Gaussian diffusions into a uniformly doped wafer of opposite type. (Profiles for three surface concentrations are indicated by the solid lines and open circles. Other profiles, indicated by open squares and open triangles, result when incorrect values for the background doping density are used in the junction C-V algorithm. Points connected by the short curved lines were derived from the same C-V pairs.)

a layer diffused into homogeneous material such as bulk silicon or a sufficiently thick epitaxial layer. Such a profiling method has the significant advantage over other profiling methods that it is nondestructive and can be used to analyze junctions found in production. To obtain a doping profile from junction C-V measurements requires a complete knowledge of the doping profile on one side of the junction [5]. When profiling a diffused layer, this requirement necessitates a knowledge both of the background doping density in the original material and of the diffusion tail on the lightly doped side of the junction.

The sensitivity of the doping profile to the background doping density was studied by generating theoretical C-V data which was treated using a profile algorithm [6] to produce a diffused layer profile. The diffusions were assumed to be Gaussian with a surface concentration of 10^{16}, 10^{17}, or 10^{18} cm^{-3}. The junction depth was taken as 1 μm and the background doping density as 10^{15} cm^{-3}. The three diffused layer profiles are shown as solid curves in figure 1. The figure also illustrates the effect of incorrectly estimating the background doping density. Note that a 1 percent error in this estimate causes significant errors in the profile at the higher diffused layer doping densities.

For the diffused layers with surface concentrations of 10^{17} and 10^{18} cm^{-3}, the plotted points represent theoretical C-V data over the range from 0.3 V applied forward bias to 90 V applied reverse bias. For the diffused layer with surface concentration of 10^{16} cm^{-3}, the range was from 0.3 V applied forward bias to 22 V applied reverse bias, at which point the space-charge region depleted completely through the diffused layer. For the analysis the built-in voltage was assumed to be 0.7 V.

This preliminary analysis indicates that determination of diffused layer profiles requires highly accurate knowledge of the background doping density. At present it appears that if the background doping density is known to within 1 percent, the practical range over which one can profile a diffused layer is limited to doping densities up to 30 times the background doping density. In this range the true value of the diffused layer doping density is within a factor of two of the value determined from C-V measurements. (R. L. Mattis and M. G. Buehler)

Plans: The multilaboratory test to examine the stability of the resistivity wafer standards will be designed and initiated. Generation of additional sets of wafer standards will proceed as necessary to meet demand. Requests for other types of standard reference materials related to characterization of semiconductor silicon will be considered as received from various sources with a view to the generation of the appropriate standard material. A small test among several interested laboratories will begin under the auspices of ASTM Committee F-1 to test a proposed recommended practice for setting probe force on four-probe arrays.

Spreading resistance efforts will concentrate on understanding the disparity in the *p*-type calibration curve already generated, generating an *n*-type silicon calibration curve, and beginning a study of the effect of various measurement variables on the accuracy and stability of spreading resistance measurements.

A study of the effects of various measurement parameters on the measurement of sheet resistance of epitaxial layers by the four-probe method will begin shortly. This study is similar to the study recently completed on bulk wafers (NBS Tech. Note 773, pp. 43-49).

Various aspects of junction C-V doping profiles will be studied with regard to profiles at various gate biases, profiles at forward biases, profiles of large and small junctions, and diffused layer profiles.

3.2. GENERATION-RECOMBINATION-TRAPPING CENTERS

Objective: To develop electrical measurement methods for characterizing the electronic properties and density of generation-recombination-trapping (GRT) centers in silicon with emphasis on methods applicable to control of parameters such as lifetime and junction leakage current.

Progress: A simplified apparatus for measuring thermally stimulated properties of a *p-n* junction was constructed and tested. It has both a fast thermal cycle time and a rapid sample throughput, and it is inexpensive. The thermally stimulated

current of a gold-doped p^+n junction was found to display a distinct peak, confirming earlier theoretical predictions.

Simplified expressions for finding the carrier lifetime in diodes with various base width from reverse recovery measurements were evaluated and shown to be applicable in the transition region where the base width is about equal to the diffusion length. Surface photovoltage lifetime measurements were successfully made on an epitaxial n/p wafer with n^+ pockets diffused at the n/p interface by limiting the measurements to wavelengths which do not penetrate the epitaxial layer.

Computer print-out tables of resistivity of gold-doped silicon as a function of gold density were prepared.

Thermally Stimulated Properties — An inexpensive apparatus was constructed for measuring the thermally stimulated current and capacitance of p-n junctions. The apparatus, pictured in figure 2, was designed to facilitate the electrical characterization of a p-n junction mounted in a 10-pin, TO-5 header. The junction, pictured in figure 3, is mounted on a ceramic chip which isolates the junction from the header. Also mounted on the chip is a temperature sensing diode which is electrically isolated from the junction under test.

In operation, the TO-5 header is inserted into the thermal transfer block, the cap is raised into position and the chamber is evacuated by a mechanical pump. Liquid nitrogen, introduced at the funnel, flows into the bellows where it cools the thermal transfer block to the initial temperature. This block is heated by a 150-W heater, silver soldered into the center of the block. The stainless steel bellows allows for thermal expansion of various parts and keeps the block pressed firmly against the TO-5 header.

Initial tests indicate that the system covers the temperature range from 82 to 673 K (400°C) and has a maximum heating rate of 9.3 K/s, a capacitance resolution of 10^{-15} F, and a current resolution of 10^{-14} A. To minimize degradation of measurement accuracy, lead length to measuring instruments is less than 30 cm.

(M. G. Buehler and A. W. Stallings)

The capabilities of this system were demonstrated by use of a gold-doped p^+n junction. The n-region of the junction is an epitaxial layer with a nominal resistivity of 10 Ω·cm and a nominal thickness of 12.5 μm. The p^+ region has a nominal sheet resistance of 80 Ω/□ and is 20 mils (0.51 mm) in diameter. The p^+n junction is nominally 1 μm deep. Gold was evaporated on the back side of the slice and was diffused for 24 hours at 800°C to obtain a density of approximately 10^{13} cm^{-3}. The dynathermal current and capacitance were measured at a reverse bias of 20 V with several heating rates. The results are shown in figure 4. Two traces are shown for

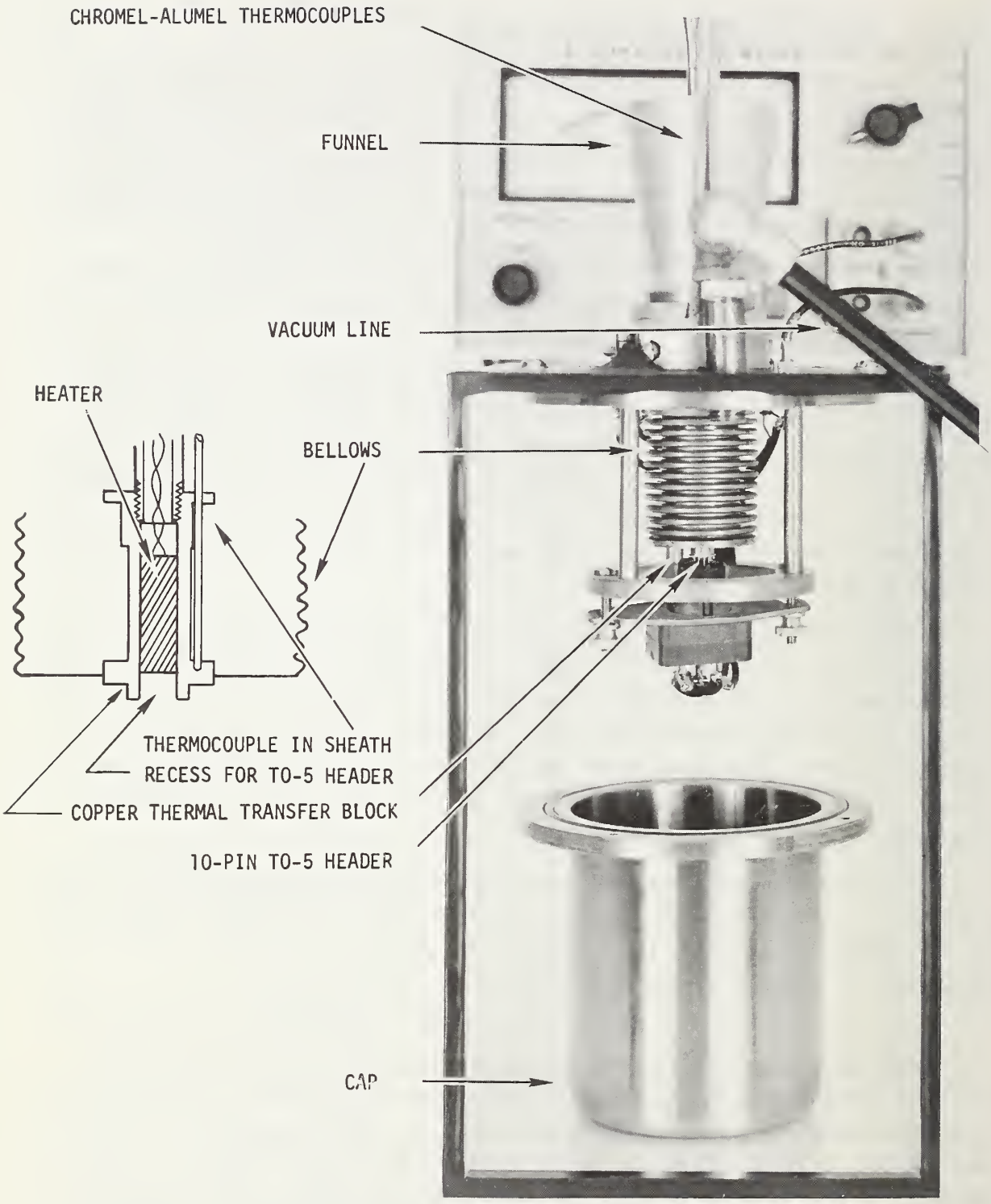

Figure 2. A simple apparatus for measuring the thermally stimulated current and capacitance of p-n junctions. (The inset shows details of the heater assembly.)

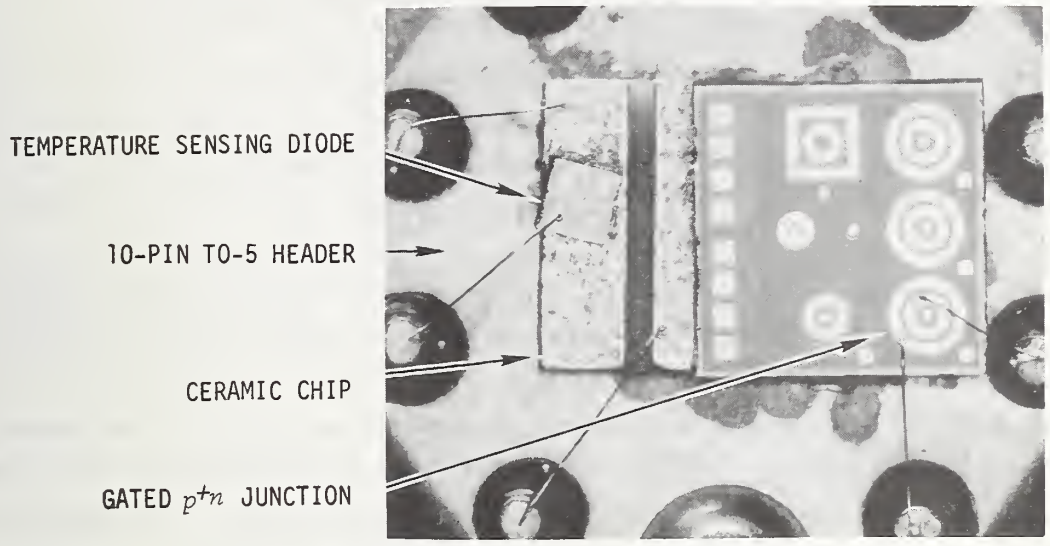

Figure 3. Test junction mounting configuration.

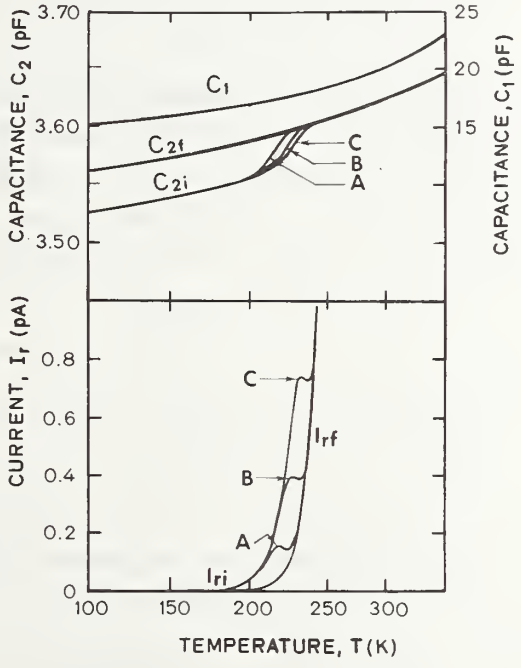

Figure 4. Dynathermal measurements of the gold acceptor on the n-side of a p^+n junction. (Heating rates: 1.6 K/s, curves A; 4.8 K/s, curves B; and 9.3 K/s, curves C; Device No. 2107.1.)

each measurement. One, labeled C_{2i} or I_{ri}, was taken in the fully charged condition in which all the gold centers are occupied by an electron, and the other, labeled C_{2f} or I_{rf}, was taken in the steady state condition where the fraction of gold centers occupied by an electron is governed by the relative magnitudes of the electron and hole emission rates, which are given respectively by [1]:

$$e_n = 1.97 \times 10^7 \, T^2 \exp(-0.547/kT), \text{ and}$$

$$e_p = 5.82 \times 10^6 \, T^2 \exp(-0.590/kT),$$

where k is Boltzmann's constant, 8.6171×10^{-5} eV/K, and T is the absolute temperature. In the steady state condition, most of the gold centers are not occupied by an electron.

The defects were charged by zero biasing the junction at 82 K. The peaks in the current responses shown in figure 4 for the fully charged condition occur at emission temperatures of 220, 230, and 235 K depending on the heating rate. The emission temperature and heating rate identify gold as the defect center [2].

The gold density, N_t, was computed from [3]:

$$N_t = \frac{2(V_2 - V_1) \, C_1{}^4 (C_{2f}{}^2 - C_{2i}{}^2) \, (e_n + e_p)}{q\varepsilon A^2 (C_1{}^2 - C_{2f}{}^2) \, (C_1{}^2 - C_{2i}{}^2) \, e_n}$$

where q is the electronic charge; ε is the dielectric constant of silicon; A is the junction area; C_1 is the capacitance of the junction, measured at zero bias; C_{2f} and C_{2i} are capacitances of the junction, measured at a reverse bias of 20 V in the steady state and fully charged conditions, respectively; and e_n and e_p are the electron and hole emission rates, respectively. From data in the temperature range from 82 to 200 K, the gold density is found to be approximately 1.5×10^{13} cm^{-3}. The general shape of the current curve, I_{ri}, for the gold initially charged shown in figure 4 was predicted theoretically in a previous publication [4]. A distinct peak appears in the current response. This occurs for a defect center, such as the gold acceptor in an *n*-type region, for which the electron emission rate is significantly larger than the hole emission rate. This response is different from that of the process-induced defect [2] for which the hole and electron emission rates are nearly equal and where a peak was not visible. Such differences provide excellent clues in deciding the nature of a defect center. Note that once electrons are released from the gold acceptor, the junction begins to leak. This indicates that the gold acceptor is responsible for the leakage of this junction. (M. G. Buehler and W. E. Phillips)

Diode Recovery Methods — Work was completed on development and analysis of approximate expressions to relate the minority carrier lifetime, τ, to the storage

time, t_s, of thin base diodes. Earlier work (NBS Tech. Note 754, pp. 10-12) showed that the traditionally used approximation [5]:

$$\operatorname{erf}\sqrt{t_s/\tau} = [1 + (I_r/I_f)]^{-1}, \tag{1}$$

where I_f is the forward current and I_r is the reverse current, is valid when the base width, the distance from the edge of the space charge region to the contact on the more lightly doped side of the junction, is greater than three diffusion lengths.

For shorter base diodes the series developed by Byczkowski and Madigan [6] (NBS Tech. Note 788, p. 15) should be used; however, because of the complexity of this complete relationship, eq (1) is frequently employed in circumstances where it is not valid. To alleviate this problem, two simplified approximations to the complete relationship were evaluated as a function of the ratio of base width, W, to the diffusion length, L, (normalized base width) and the ratio of forward to reverse current.

The zeroth order approximation is based on the derivative of the first term of the series with respect to storage time (NBS Tech. Note 788, p. 18):

$$\tau_0 \approx \left\{ \frac{d}{dt_s} \left[\ln \left(1 + \frac{I_f}{I_r} \right) \right] - \frac{\pi^2 D}{4W^2} \right\}^{-1}, \tag{2}$$

where D is the minority carrier diffusion coefficient.

In some circumstances the succeeding terms in the series do not become small enough fast enough. In this situation it is advantageous to use the first two terms of the series to obtain a first order approximation. This can be done by using an iterative approach to calculate the lifetime; first, τ_0 is computed using eq (2), and then a correction derived from the second term in the series is computed. One then obtains

$$\tau_1 \approx \tau_0 + \tau_c , \tag{3}$$

where

$$\tau_c \approx 8\tau_0 A^2 \frac{(1 + A^2)}{(1 + 9A^2)} \exp\left[- \frac{8A^2 t_s}{\tau_0} \right], \tag{4}$$

$A = (\pi L_0/2W)$, and $L_0 = \sqrt{D\tau_0}$.

The error introduced by computing the minority carrier lifetime with eqs (1), (2), and (3) was computed as a function of the normalized base width for four different current ratios. The percent error, ε, ε_0, or ε_1, was defined as

$$\varepsilon_i \equiv \left[1 - (\tau_i/\tau_{true}) \right] \times 100, \tag{5}$$

where τ_{true} is the lifetime computed from the full series and τ, τ_0, or τ_1 was computed using eq (1), (2) or (3), respectively. The derivative required for τ_0 was

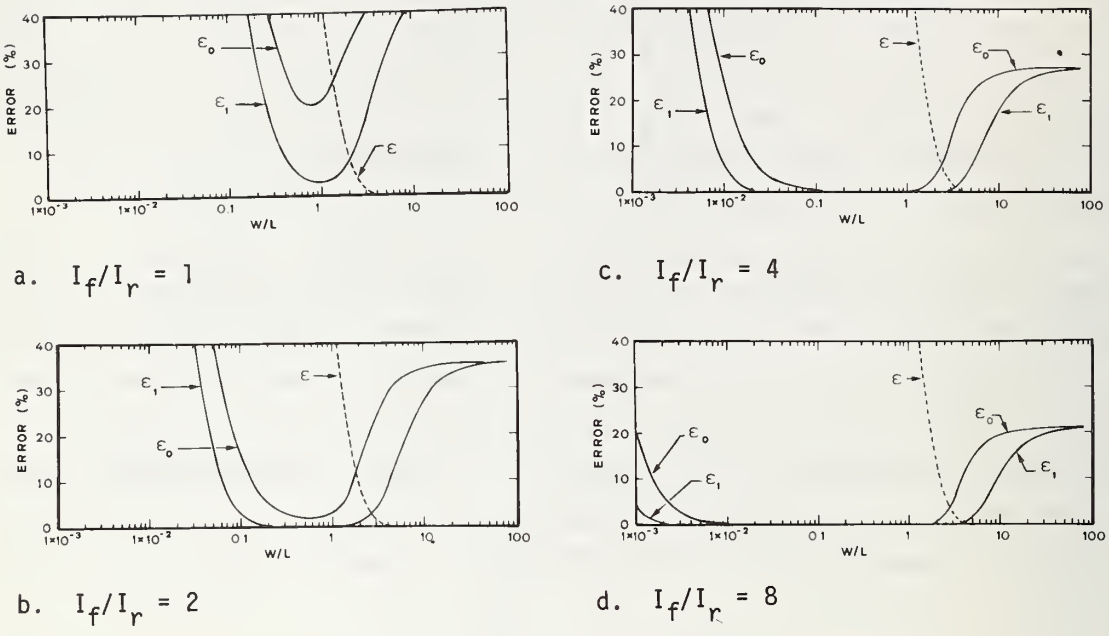

Figure 5. Error, ε, ε_0, or ε_1, introduced by using eqs (1), (2), or (3), respectively, to compute the minority carrier lifetime from diode storage time for various values of the ratio of forward to reverse current (I_f/I_r). (The error is plotted as a function of the ratio of base width to diffusion length (W/L).)

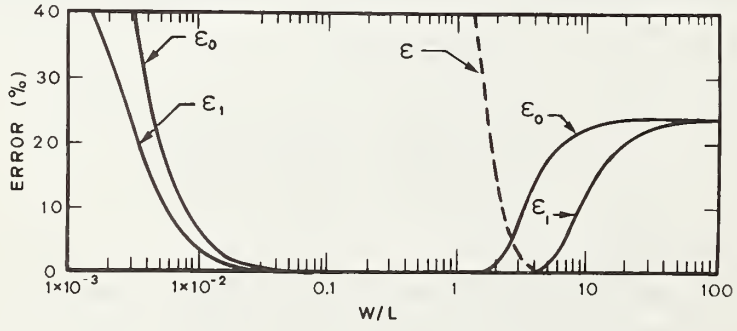

Figure 6. Error, ε, ε_0, or ε_1, introduced by using eqs (1), (2), or (3), respectively, to compute the minority carrier lifetime from diode storage times for I_f/I_r = 4 and I_f/I_r = 8. (The error is plotted as a function of the ratio of base width to diffusion length (W/L).)

computed from the change in the current ratio caused by an incremental change in the storage time. The results of the calculations are shown in figure 5.

The errors associated with eqs (2) and (3) decrease as the current ratio increases. An increase in the current ratio causes an increase in the normalized storage time. Since the terms of the approximated series converge as $\exp(-8nA^2t_s/\tau)$, where n is the term number, τ_0 and τ_1 become more accurate approximations to the series as the current ratio increases.

Neither τ_0 nor τ_1 is a good approximation to the minority carrier lifetime when the normalized base width is large. For wide base diodes ($W/L > 3$) the storage time is independent of W/L. Hence, as the normalized base width increases, the arguments of the exponents in the series expansion become small and the series converges too slowly to be approximated by its first few terms.

The approximations τ_0 and τ_1 break down at very short base widths because the normalized storage time decreases roughly as the square of the normalized base width in sufficiently thin diodes. In this case the series again cannot be adequately approximated by its first or first and second terms.

In an experimental situation, the derivative normally would be estimated from relatively large finite differences rather than incremental measurements. As an example of such a case, the errors associated with computing the lifetime from the storage times for $I_f/I_r = 4$ and $I_f/I_r = 8$ were calculated as a function of the normalized base width. The mean of the two storage times was used in eq (4) to calculate τ_c and in eq (1) to calculate τ. The results are shown in figure 6.

Since the errors associated with eqs (1), (2), and (3) are all positive, the approximations underestimate the lifetime. The best estimate for the lifetime is obtained from the approximation which gives the largest value.

One difficulty with the application of these simple approximations is that they become very sensitive to measurement error at small values of normalized base width. For example, in the case of τ_0, the lifetime is the reciprocal of the difference of two nearly equal numbers. Thus, any small error in the determination of the base width, storage time, diffusion constant, or the current ratio results in a large error in the computer lifetime. On the other hand, the utility of these approximations is that they can be used to compute the minority carrier lifetime associated with diodes whose normalized base width is in the transistion region between the short and long base extremes. (D. C. Lewis)

Surface Photovoltage Method — Preliminary surface photovoltage (SPV) measurements on an epitaxial *n/p* wafer with n^+ pockets diffused at the *n/p* interface indicate

that reasonable lifetime values can be obtained by covering only the wavelength range for which essentially all incident light is absorbed in the epitaxial n-layer. The plot of intensity as a function of reciprocal absorption coefficient for a 12-μm thick epitaxial layer of the above wafer showed a linear region between 0.7 and 0.8 μm and an upturn beyond 0.8 μm caused by light penetrating the n^+ pockets and the p-type substrate. The linear region could be extended by measurements at even shorter wavelength, but this entails a grating change in the monochromator. (W. R. Thurber)

Gold-Doped Silicon — Computer print-out tables were generated which give the resistivity of silicon as a function of gold density for a range of boron or phosphorus densities from 1×10^{13} to 1×10^{17} cm^{-3}. The equations and parameters used in the calculations have been given previously (NBS Tech. Note 788, pp. 18-23). However, the lattice and ionized impurity mobilities were combined by the sine and cosine integral method [7] rather than the reciprocal method used previously. As discussed in Section 3.3., the integral method of combining mobilities improves slightly the agreement between theory and experiment for resistivity as a function of gold density for silicon crystals with initial resistivity of less than 1 Ω·cm, but significant discrepancies still remain. Copies of the tables are available on request. (W. R. Thurber and W. M. Bullis)

Plans: Measurements of thermally stimulated properties will be employed to characterize various heavy metals such as copper and iron and to study the effect of diffused phosphorus getters on defect concentrations. Defect densities will be profiled by various low temperature C-V methods.

Further work on diode recovery measurements will be deferred indefinitely; work on a draft method for measuring surface photovoltage will be completed. Hall effect and resistivity measurements will be continued as a function of temperature to obtain further data on the energy levels of gold in silicon.

3.3. CARRIER MOBILITY

Objective: To determine values of the electron and hole mobilities as a function of resistivity and impurity density in silicon which is uncompensated or only lightly compensated and to develop appropriate expressions to calculate values of mobility which agree with experimental data.

Background: It was noted in previous work [1] (NBS Tech. Note 788, pp. 23-24) that the computed doping densities for low resistivity silicon crystals (<1 Ω·cm) were lower than those obtained experimentally [2]. This difference occurred in part because of difficulties with the calculation of ionized impurity and mixed mobilities.

Experimentally, recent data on the mobility of holes as a function of impurity density [3] is in disagreement with earlier work [2, 4]. The mobility section of ASTM Commitee F-1 on Electronics has noted that discrepancies exist in the data and is working to resolve some of the uncertainties. Of mutual interest is the goal of obtaining appropriate expressions which can be used with confidence by the electronics industry to relate mobility to impurity density and resistivity.

Progress: To summarize the existing situation theoretical calculations of conductivity mobility as a function of impurity density were compared with experimental results for boron- and phosphorus-doped silicon [3, 4]. As shown in figures 7 and 8 the calculated mobility was found to be somewhat larger than the experimental data, especially at the higher impurity densities.

The calculated mobilities were obtained by combining the effects of lattice and ionized impurity scattering. The lattice mobility, μ_L, was based on the results of Ludwig and Watters [5] and the Brooks-Herring [6] formula was used for the calculation of impurity mobility, μ_I. Conductivity effective masses of 0.30 and 0.33 times the free electron mass, for electrons and holes, respectively, (based on data of Barber [7]) were used in the impurity mobility calculation. For the calculated curves the resultant mobility, μ, was obtained by combining the lattice and impurity mobilities by the reciprocal method ($1/\mu = 1/\mu_L + 1/\mu_I$) or by the sine-and-cosine-integral method [8]. The integral method is more accurate from a theoretical viewpoint and results in lower values of mixed mobility particularly in the region where both lattice and ionized impurity scattering are important. The curves are not plotted for impurity densities greater than about 5×10^{18} cm^{-3} as the Born approximation used for the calculation of impurity mobility no longer applies and Boltzman statistics are not valid.

Curve 1 in figure 7 is an empirical one derived by Caughey and Thomas [4] to fit Irvin's data for electron mobility [2]. Curve 2 was calculated by the reciprocal method for phosphorus as the dopant with a constant activation energy of 0.044 eV [9] with respect to the conduction band edge. Curves 3 and 4 were calculated by the sine-and-cosine-integral method. For these curves, the activation energies of phosphorus were taken as 0.044 and 0.000 eV respectively; the latter choice gives the maximum change which would occur as a result of decreasing activation energy at large impurity densities [8].

It is evident that the gap between the calculated mobility and the empirical curve widens as the impurity density increases. Rode [10], in similar calculations, also found that the experimental mobility data fell further below his calculated curves as the impurity density increased. He attributed this to the failure of the spherical band approximation to accurately describe the ionized impurity scattering.

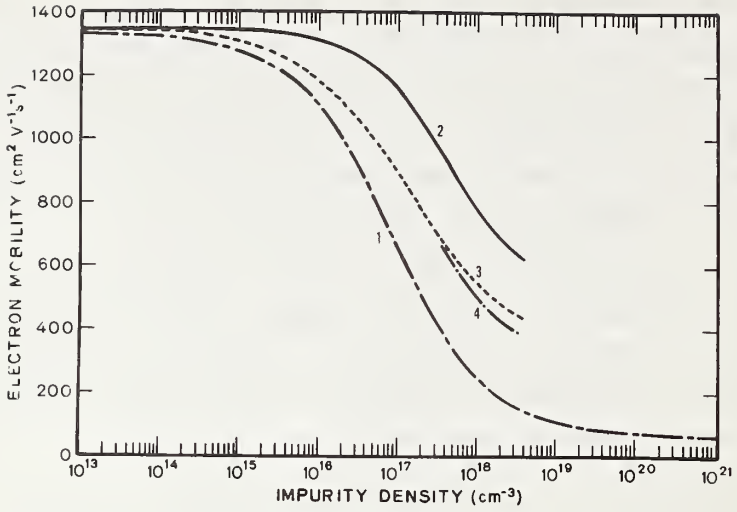

Figure 7. Conductivity mobility of electrons at 300 K as a function of impurity density. (See text for identification of curves.)

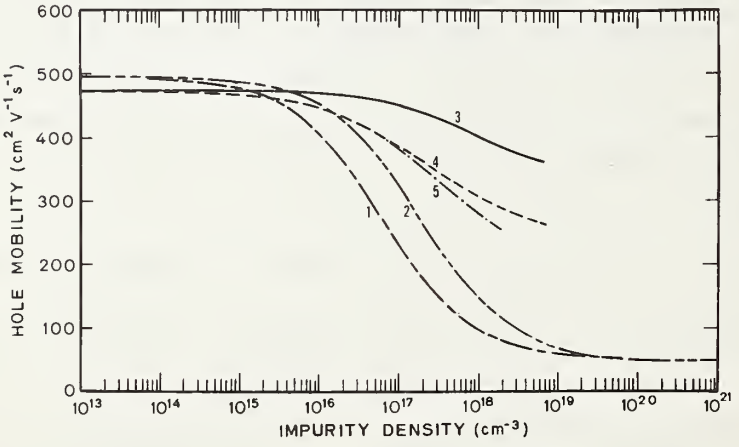

Figure 8. Conductivity mobility of holes at 300 K as a function of impurity density. (See text for identification of curves.)

Two empirical curves of hole mobility are given in figure 8. Curve 1, as before, was derived by Caughey and Thomas [4] to fit Irvin's data for hole mobility [2]. Curve 2 is based on data obtained by Wagner [3] on boron-implanted silicon. These two empirical curves differ significantly in the range of impurity density from 10^{16} to 10^{19} cm^{-3}. Curve 3 was calculated by the reciprocal method for boron as the dopant with a constant activation energy of 0.045 eV [9] with respect to the valence band edge. Curves 4 and 5 were calculated by the sine-and-cosine-integral method for boron activation energies of 0.045 and 0.000 eV, respectively. The calculated hole mobility deviates considerably from both empirical curves at impurity densities for which ionized impurity scattering is important. (W. R. Thurber and M. G. Buehler)

Plans: Additional scattering mechanisms, such as carrier-carrier scattering, and refinements in ionized impurity scattering will be considered in calculations of mobility. More extensive comparisons of calculated and experimental mobilities will be made.

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4. SEMICONDUCTOR PROCESS CONTROL

4.1. DIE ATTACHMENT EVALUATION

Objective: To evaluate methods for detecting poor die attachment in semiconductor devices with initial emphasis on the determination of the applicability of thermal measurements to this problem.

Progress: Further computations using the TRUMP [1] thermal analysis computer program were undertaken using boundary conditions appropriate to a round silicon chip on an infinite heat sink. Because of the good correlation achieved between the computer solutions and analytical solutions based on this simple model (see 5.1.), it was decided that the computer analysis of heat flow in a more complex structure to determine the limitations of thermal response techniques for detecting poor die adhesion in diodes could be resumed.

The structure shown in figure 9 was used to approximate the true TO-5 header-chip structure of the diodes previously investigated (NBS Tech. Note 727, p. 26). Cylindrical symmetry was assumed for modeling purposes. The approach taken in the modeling of this device is one of using successively finer subdivisions (nodes) until no appreciable difference in the required temperature is found [2]. The average junction temperature computed 50 μs after the termination of the 10-ms heating power pulse was found to be within 1°C of the measured value, but when the average junction temperature was measured 50 μs after the steady state power was terminated, the computed temperature was found to be approximately 5°C above the measured value. A study of the data generated by the computer has indicated that further modeling changes are needed to describe the mesa diode adequately.

(F. F. Oettinger and R. L. Gladhill)

Long-term, single-operator measurements of steady-state and transient thermal response, to check the repeatability that can be achieved with the transistor die attachment evaluation equipment, were completed. Twenty-six sets of measurements were made on two control transistors (Device Nos. 6 and 10, Lot AT) without voids and 25 sets of measurements were made on two transistors with 40-percent void areas (Device Nos. 3 and 10, Lot ATV) over a period of 7 weeks. For the measurements, the test device was mounted on a temperature controlled heat sink held at 25°C. The emitter-base voltage, V_{EB}, was measured first under conditions of negligible internal power dissipation and then at some specified time, t_{meas}, after the termination of a 5-ms long heating power pulse. A quantity proportional to the junction-to-case temperature difference was obtained by subtracting the second voltage from the first. Both transient and steady state thermal response measurements were made 10, 50, and

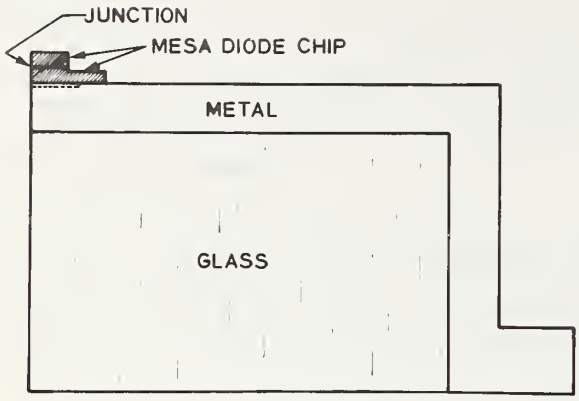

Figure 9. Cross sectional view of structure used to approximate a mesa diode chip on a TO-5 header.

100 μs after the heating power pulse was terminated. Transient thermal response measurements were also made 10 μs after the heating power pulse was terminated with the devices mounted in a standard socket rather than in the heat sink. The heating current and voltage for the transient measurements were 150 mA and 10 V, respectively, while for the steady-state measurements they were 50 mA and 10 V, respectively.

The results are summarized in table 2. Each entry represents the average value ± the pooled sample standard deviation. In each block of data the first line is the thermal response of devices without voids in the die attachment, the second line is the thermal response of devices with 40-percent void area in the center of the die, and the third line is the increase in response of devices with voids over that of devices without voids expressed as a percentage of the latter.

For the data in the first three columns, the case temperature is that of the heat sink; for the data in the fourth column, the case temperature was assumed to be that of the room ($\sim 24^{\circ}C$). Comparison of columns 1 and 4 indicates that it is not necessary to mount the device under test in a temperature controlled heat sink.

The last column gives data for the change in temperature sensitive parameter, V_{EB}. Comparison of this column with columns 1 and 4 suggests that information regarding voids can be obtained directly from the V_{EB} difference without the necessity of converting the results to a temperature difference.

Data in the first three columns suggest that the sensitivity of the measurement to the presence of voids is nearly constant during the first 100 μs after the termination of the heating power pulse. This is due to the fact that the initial rate of cooling of a device with a void is nearly the same as that of the control. The optimum delay is dependent in part on the smallest size void to be detected; experience has shown that a delay time of 50 μs is appropriate for the range of voids used in this study.

Table 2 — Results of Long-Term, Single-Operator Measurements of Thermal Response

	Temperature Controlled Heat Sink			Standard Socket	
	ΔT_{JC}, °C			ΔT_{JA}, °C	ΔV_{EB}, mV
t_{meas} =	10 μs	50 μs	100 μs	10 μs	10 μs
Steady state measurements:					
No void	30.3±0.5	29.4±0.4	28.9±0.4		
40% void	32.1±0.4	31.2±0.4	30.6±0.4		
% increase	6 ±2	6 ±2	6 ±2		
Transient measurements:					
No void	21.4±0.3	18.8±0.3	17.3±0.3	21.9±0.4	47.1±0.8
40% void	30.0±0.3	27.3±0.3	25.5±0.3	30.6±0.5	65.0±1.1
% increase	40 ±2	45 ±2	48 ±3	39 ±3	38 ±3

The maximum pooled sample standard deviations for the steady-state and transient thermal response measurements (0.5°C) lie within an acceptable range for the instrument and mounting fixtures in the present application. Also, it should be noted that the sample standard deviations are slightly less than those reported previously for single measurements on many devices with the same size void (NBS Tech. Note 773, p. 23; cf. last column, table 2.) (R. L. Gladhill and F. F. Oettinger)

Plans: The analysis of heat flow to determine the limitations of thermal response techniques for detecting poor die adhesion in diodes will continue using the TRUMP thermal analysis computer program. Power transistors will be bonded with various size controlled voids on TO-66 headers, and thermal response measurements will be made to determine their sensitivity to voids in the die adhesion in this size package.

4.2. INTERCONNECTION BOND EVALUATION

Objective: To survey and evaluate methods for characterizing interconnection bond systems in semiconductor devices and, where necessary, to improve existing methods or develop new methods in order to detect more reliably those bonds which will eventually fail.

Progress: The resolution-of-forces equations were used to calculate the effects on the measured pull strength of ultrasonic wedge bonds which occur when the pull test parameters are varied over a range of values similar to that which might be obtained

in industrial use. The results for a typical example indicate that the pull angle ϕ must be controlled to within 10 deg if the reproducibility of the test is to be better than 30 percent, but other parameters need not be so well controlled.

Feasibility studies have shown that aluminum ribbon wire can be ultrasonically bonded to copper thick film substrates. The vibration modes of two long bonding tools were studied during bonding. A study of beam-lead bonding tests was begun. A phase-locked-loop ultrasonic bonding power supply was characterized and certain instabilities identified. Pull test specifications were prepared for large diameter aluminum wire. Studies of the bonding characteristics of fine gold wire were initiated.

Pull Test Evaluation — The sensitivity of the measured pull strength of wire bonds to variations in experimental conditions was analyzed for the case, appropriate to unannealed aluminum ultrasonic wedge bonds, in which resolution of forces applies [1]. The normalized variation in pull strengths of the bond to the terminal, $\Delta F(t)$, and of the bond to the pad on the die, $\Delta F(d)$, were studied as a function of the position of the pulling hook, α; the loop height above the terminal post, h; the height of the terminal post above the die, H; the bond-to-bond spacing, d; and the pull angle with respect to the normal to the substrate, ϕ. The equations used to make the calculations have been reported previously [2].*

To illustrate the application of this analysis, computations were made for a transistor in a TO-18 can.† Each of the five quantities was varied about its nominal value while the other four quantities were held constant, and $\Delta F(t)$ and $\Delta F(d)$ were computed. The results are summarized in table 3; the quantities are listed in order of decreasing effect on the measured pull strength. Except for variation of ϕ, the variation is expressed in percent of the nominal value.

It can be seen that, for the device described, the pull angle ϕ has the greatest effect on $\Delta F(t)$ and $\Delta F(d)$. Of the five parameters, the pull test operator controls only ϕ and α; the reproducibility of h and d is dependent on the bonding machine, and that of H is dependent on the header lot and die thickness. In making wire bonds in this laboratory, h and d can be reproduced to ±3 and ±3.8 percent (one standard deviation), respectively. Typical manufacturer's specifications for headers suggest that variations in post height of ±30 percent may be expected. An estimate of the overall variation to be expected in determining pull strength was obtained by calculating

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*A listing of the BASIC computer program used for these calculations is available on request.

†This device was previously studied in connection with thermal flexure problems (NBS Tech. Note 717, pp. 23-25). Nominal values assumed were taken as: $\alpha = 0.5$; h = 12.0 mils (0.3 mm); H = 5.0 mils (0.13 mm); d = 40.0 mils (1.02 mm); and $\phi = 0$ deg.

Table 3 — Dependence of $\Delta F(t)$ and $\Delta F(d)$ on Pull Test Conditions for a TO-18 Transistor

Quantity	Change	$\Delta F(t)$	$\Delta F(d)$	Change	$\Delta F(t)$	$\Delta F(d)$
ϕ	+10 deg	-11%	+14%	+20 deg	-19%	+37%
	-10 deg	+20%	-8%	-20 deg	+50	-13
d	+10%	-7%	-6	+20%	-13	-11
	-10%	+8%	+6	-20%	+16	+13
h	+10%	+5%	+5	+20%	+11	+10
	-10%	-5	-5	-20%	-12	-10
α	+10%	+4	-3	+20%	+9	-5
	-10%	-3	+4	-20%	-6	+9
H	+10%	+2	+0.5	+20%	+3	+1
	-10%	-2	-0.5	-20%	-3	-1

values of $\Delta F(t)$ and $\Delta F(d)$ as a function of ϕ for two cases for the sample device. In one case each of the other four quantities assumed its smallest value, in the other each assumed its largest value. The results for these simulations of the application of the pull test in an industrial environment, shown in figure 10, indicate that, depending on the mode of bond failure, variations in ϕ of 10 deg can produce differences in pull strength from the zero degree case of as much as 30 percent.

(A. H. Sher)

Ribbon Wire Bonding Technology — In response to the desire of the industry to reduce costs by decreasing the quantity of gold used in microelectronic devices, ceramic substrates with thick films of copper and nickel have become commerically available; the feasibility of ultrasonically bonding aluminum wire directly to such films was studied using 38 by 13 μm (1.5 by 0.5 mil) aluminum ribbon wire. Single-level bonds were made to the films as received; no special cleaning or etching was performed. The loop height was 15 mils (0.8 mm) and the bond-to-bond spacing was 60 mils (1.52 mm). In each case, the bonding force was 25 gf (0.24 N). The numerical value of the results obtained can be expected to vary with equipment used. For the bonder at NBS, the strongest bonds to the copper films were obtained with a bonding time of about 110 ms and a tool tip vibration amplitude of about 35 μin. (0.9 μm); those to the nickel films were obtained with a bonding time of about 180 ms and a tool tip vibration amplitude of about 40 μin. (1.0 μm). Bonds made to copper thick films exhibited pull strengths in the range of 7 to 10 gf (69 to 98 mN); bonds made

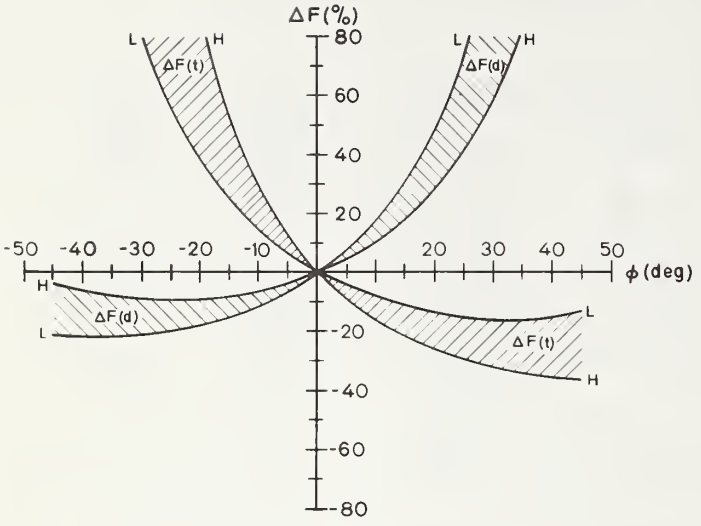


Figure 10. Normalized variation in measured pull strength for the terminal bond, ΔF(t), and die bond, ΔF(d) as a function of pull angle ϕ.

(For case L:
d = 38.5 mils (0.98 mm);
h = 11.6 mils (0.29 mm);
α = 0.375; and
H = 3.5 mils (0.09 mm).
For case H:
d = 41.5 mils (1.05 mm);
h = 12.4 mils (0.31 mm);
α = 0.625; and
H = 6.5 mils (0.17 mm).)

to the nickel thick films showed pull strengths about one-half those made to the copper films. (H. K. Kessler)

Studies of Ultrasonic Bonding Tools — The in-process monitoring technique, applied last quarter to the study of short bonding tools (NBS Tech. Note 788, pp. 35-41), was used to study the modal patterns of long bonding tools while bonding 1-mil (0.25-mm) diameter aluminum (1% silicon) wire. A fixed-tuned ultrasonic power supply was used to drive the transducer. Two bonding tools, 0.828-in. (21.0-mm) long, were studied. One was made of tungsten carbide, and the other was made of titanium carbide; both tools were of conventional design.

The modal patterns were measured for the free vibration condition, in which the tools were unloaded, and for a normal bonding load of 25 gf (0.24 N) about 5 ms before the end of the 50-ms long bonding cycle. For convenience of display, both the loaded and unloaded modal patterns were normalized to a constant horn amplitude of 30 μin. (0.76 μm) peak-to-peak.

The modal patterns obtained for the long tungsten carbide bonding tool are shown in figure 11. The principal differences between this tool and the comparable short tool are the double node below the horn (NBS Tech. Note 527, pp. 32-33), the smaller rise in nodal position during bonding, and the larger vibration amplitude at the top of the tool, which results because the tool extension above the horn is approximately a quarter wavelength.

The modal patterns obtained for the long titanium carbide bonding tool are shown in figure 12. The physical characteristics of this material are quite different from

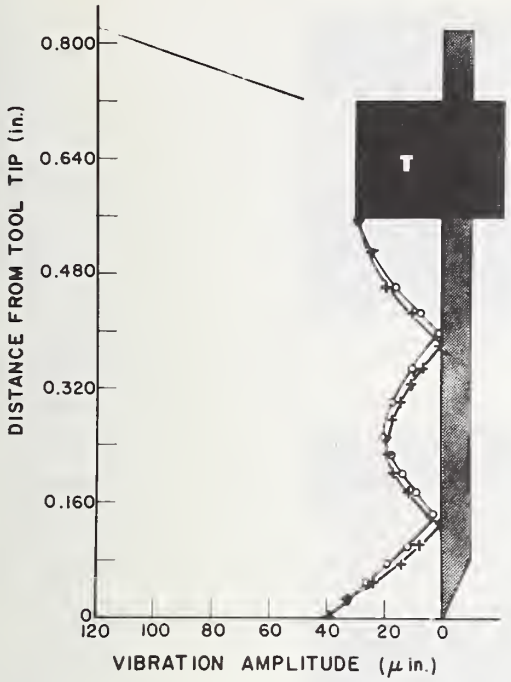


Figure 11. Modal patterns of a long tungsten carbide ultrasonic bonding tool.
(Unloaded: + .
Loaded, 5 ms before end of bonding cycle: O.
The large dark area (T) represents the position and amplitude of the transducer horn.
Note: 0.1 in. ≈ 2.5 mm; 40 μin. ≈ 1 μm.)

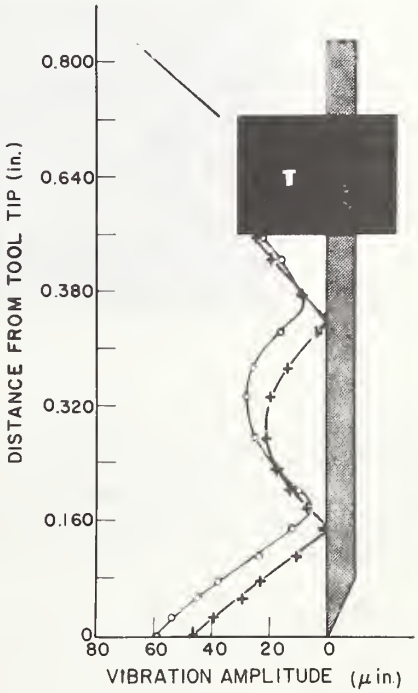
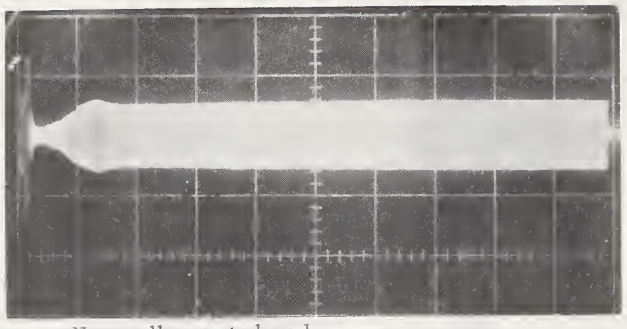
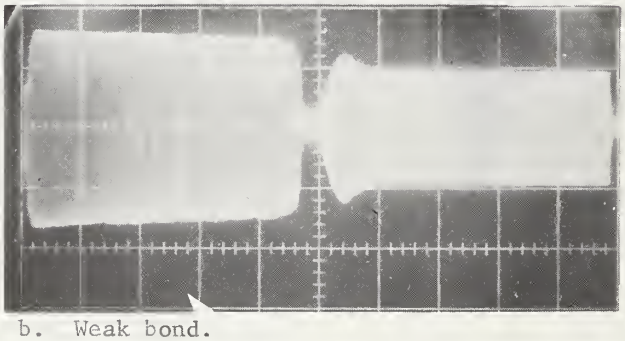


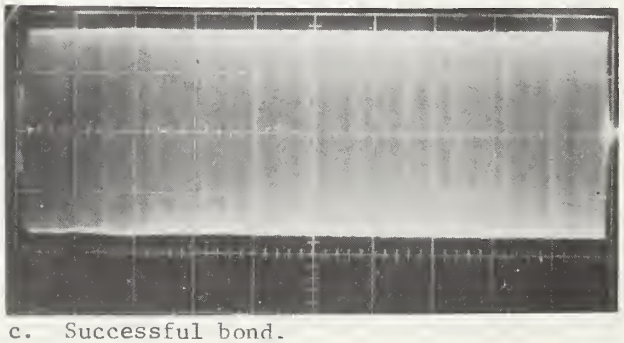
Figure 12. Modal patterns of a long titanium carbide ultrasonic bonding tool.
(Unloaded: +.
Loaded, 5 ms before end of bonding cycle: O.
The large dark area (T) represents the position and amplitude of the transducer horn.
Note: 0.1 in. ≈ 2.5 mm; 40 μin. ≈ 1 μm.)



a. Non-adherent bond.



b. Weak bond.



c. Successful bond.

Figure 13. Tool tip vibration amplitude envelopes obtained during attempted bonding with a phase-locked-loop ultrasonic power supply. (For each of the traces the coarse tuning switch was in one of the three positions that produced apparently satisfactory meter tuning under no-load (free-vibration) conditions. Horizontal scale: 20 ms/div. Vertical scale: 20 mV/div.)

those of tungsten carbide. The nodes shift more under load, and the vibration amplitude at the top of the tool is much smaller. The tool extension above the horn, although the same length as that of the tungsten carbide tool, is no longer a mechanical quarter wavelength so the amplitude at the top of the tool is similar to that at the tool tip. The upward nodal shift during bonding is not quite as great as that for the comparable short tool. The loaded node becomes broad and imprecise as on the short tool, but to a lesser extent. (G. G. Harman)

Studies of a Commercial Phase-Locked-Loop Ultrasonic Power Supply — The in-process monitoring technique was also used to study the characteristics of a 5-W ultrasonic power supply and transducer system that incorporates a self-tuning phase-locked-loop circuit to keep the system peak-tuned during bonding. Although the manufacturer no longer produces ultrasonic equipment, many of these units are in the field. This study is intended to identify problems which may be encountered by users and future designers of such equipment.

This instrument is adjusted by coarse tuning it with a panel switch to give a maximum indication on a panel meter without a load on the transducer (free-vibration condition). The unit studied could apparently be properly tuned in three of the eight switch positions. However, with a capacitor microphone placed near the tool tip, it was observed that only one of these switch positions resulted in normal power being delivered to the tool under certain actual bonding conditions. This situation was more frequently observed when using a bonding machine that required a long bonding tool rather than a short tool, and when using a bonding time of 100 ms or more.

The tip vibration amplitude envelopes for the three switch positions which produced apparently satisfactory meter tuning under no-load conditions are shown in figure 13. The bond produced by the cycle depicted in figure 13a did not adhere to the bonding pad. The bond produced by the cycle depicted in figure 13b stuck, but it lifted off with very low bond pull strength, because the phase-locked-loop became unlocked in the middle of the bonding cycle. The bond produced by the cycle depicted in figure 13c was successful.

It was also observed that when the power dial setting was changed significantly the loop became unlocked, and a different coarse tuning switch position was required to produce a satisfactory bond. Such unpredictable responses as these can lead to unreliable wire bonds.

Conversations with several users of this type of power supply indicated that these observations were not unique to the particular power supply that was studied. The reasons for such characteristics were not determined, but a few general comments are appropriate: An ultrasonic transducer is a complex electromechanical device.

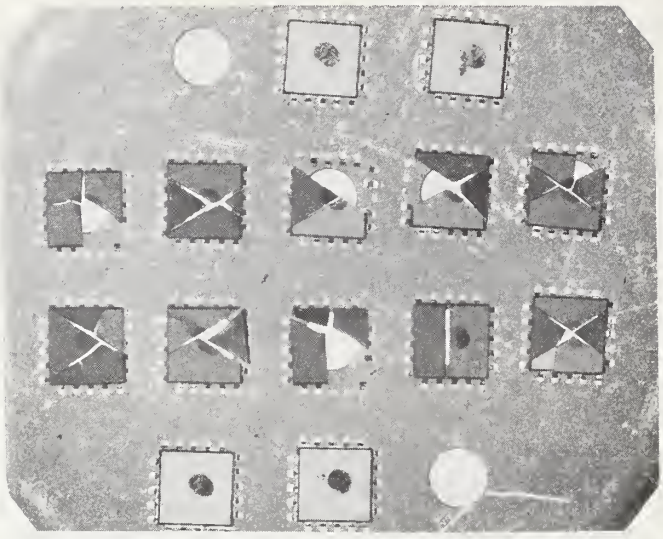


Figure 14. A portion of a ceramic bonding substrate used in beam-lead bond push-off tests. (The two middle rows contain the 10 beam-leaded dice that were subjected to the test. Four untested dice and two substrate holes are also shown. Magnification: ~ 7 X.)

There is a propagation time delay from transducer to horn to tool and back. This may change the optimum electrical V-I phase relationship during the complex varying load conditions encountered in bonding. Under these conditions, a particular locked-phase relationship may not lead to the optimum resonant frequency and vibration amplitude. In principal, at least, the self-tuning phase-locked-loop approach could offer advantages over the conventional fixed-tuned ultrasonic power supplies, particularly for large wire bonding, where the bonding forces are very high. Under such bonding conditions the mechanical resonance of the transducer-tool system may change by more than 1 kHz, detuning the system significantly. However, considering the above problems, great care in design and testing of phase-locked-loop power supplies should be carried out before manufacturing or using them. (G. G. Harman)

Beam-Lead Bond Evaluation — To assist in evaluating tests and screens for beam-lead bond integrity presently used by the industry, several companies and laboratories making or using beam-lead devices were visited. It was learned that the most commonly used destructive test is the push-off test. For this test, the dice are bonded over holes in a special substrate. A probe is pushed through the hole against a die, and the force required to break the beams or the silicon die is recorded.

In order to gain first-hand experience with this test, a wobble-tool thermocompression beam-lead bonder was obtained and set up, and several groups of beam-leaded devices were bonded on special ceramic substrates and tested by the push-off test. Typical results, illustrated in figure 14, show one of the problems with this test. In this case, ten beam-leaded dice were tested, but in all cases the silicon broke rather than the beams. Such test results are familiar to most persons in the field. The push-off force specifications are sufficiently lax that the cases in which the silicon breaks are not considered rejects. Another problem which arises in connection with this test is that it is unable to detect a few weak or unbonded beams among a large number of good ones on a die. In addition, special substrates must be used in the test rather than statistical samples of the normal product; this leads to problems of cost, sampling validity, and operator objectivity.

(G. G. Harman and H. K. Kessler)

Bond Pull Specifications for Large Diameter Wire — At the request of the Defense Electronic Supply Center a bond-pull specification for the 5- to 20-mil (0.13- to 0.51-mm) diameter aluminum wire used in JAN-TXV power transistors was developed for proposed inclusion in appropriate slash sheets to MIL-S-19500, General Specification for Semiconductor Devices. This was a difficult problem because of the many wire sizes involved (at least 10), the wide range of geometrical configurations of the transistors, and the large variety of metallurgical properties of the available wire.

In order to establish the basis for a realistic specification that offered a meaningful level of quality control and was acceptable to both users and manufacturers, five semiconductor plants were visited to obtain pull test data and other information. Two other device manufacturers contributed additional data including mean-range charts for bond pull tests, and acceptance criteria were supplied by several users. Three major bonding wire companies supplied information on tensile strength, elongation, and other relevant metallurgical data. Additional bond-pull data were obtained in-house on a variety of wire sizes in a limited selection of device types.

The specification developed covers bonds made of aluminum wire, with or without alloying additives, ultrasonically bonded to the die and either ultrasonically bonded or electrical-discharge welded to the post. The test, which is primarily for use on uncapped devices being assembled at the manufacturer's plant, is performed by placing a rounded metal hook under the span of wire midway between the two bonds and pulling vertically to destruction with the device clamped. In some cases soldered clips of copper or other material are permitted. These may also be tested by this procedure, but in this case the hook is placed as close as possible to the soldered joint on the

Table 4 — Bond Pull Limits

Wire diameter, mils (mm)	Minimum pull limit, gf (N)
1.0 (0.025)	2 (0.02)
1.3 (0.033)	3 (0.03)
1.5 (0.038)	4 (0.04)
3 (0.076)	12 (0.12)
5 (0.13)	30 (0.29)
8 (0.20)	75 (0.74)
10 (0.25)	120 (1.18)
15 (0.38)	220 (2.16)
20 (0.51)	300 (2.94)
Solder Clips	300 (2.94)

die. A bond failure is designated as any bond or wire which breaks at an applied stress less than that indicated in table 4. Procedures are included in the specification for both bond failures and die fracture.

It should be noted that, when plotted on log-log paper, the limits for large diameter wire in table 4 join smoothly with the limits for small diameter aluminum wire currently being considered for inclusion in a proposed revision to Test Method 1014, MIL-STD-883, Test Methods for Microcircuits. For completeness these small wire limits are also included in the table. (G. G. Harman)

Ultrasonic Bonding of Gold Wire — A series of experiments was begun to determine the bond strength of ultrasonically bonded gold wire and some of its alloys. Gold wire of 99.99 percent purity from one manufacturer was used for the initial tests. According to the manufacturer, the wire had a diameter of 1 mil (0.025 mm), a tensile strength of 13 gf (0.127 N), and an elongation less than 2 percent. All bonds were made on 0.9-μm thick aluminum bonding pads evaporated on a film of silicon dioxide, 0.8-μm thick, thermally grown on a silicon slice. A formal statistical set-up procedure (NBS Tech. Note 598, pp. 21-23) was carried out to establish the appropriate bonding schedule. Bonding forces of 23, 30, and 36 gf (0.23, 0.29, and 0.35 N); bonding times of 45, 70, 105, 135, and 160 ms; and eight ultrasonic tool tip vibration amplitudes in the range 20 to 85 μin. (0.51 to 2.2 μm) peak-to-peak were employed. These variations were carried out separately on both the first and the second bonds. Ten to fifteen single-level bonds, with bond-to-bond spacing of 38 to 40 mils (0.96 to 1.02 mm) and loop height of 11 to 12 mils (0.28 to 0.30 mm), were

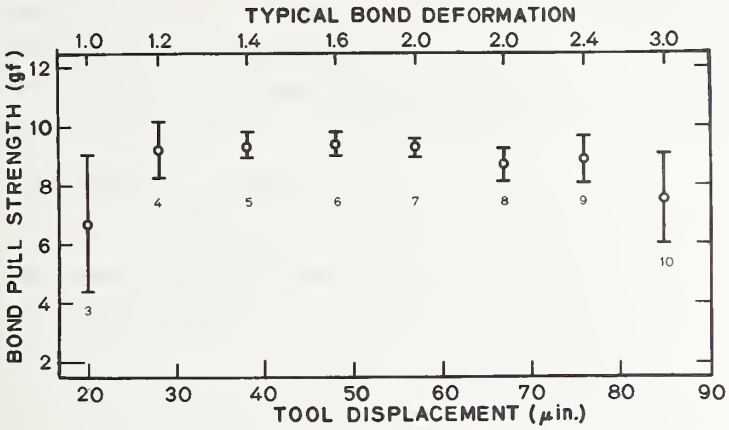


Figure 15. Bond pull strength of the first bond of an ultrasonically bonded, 1-mil (0.025-mm) diameter gold wire. (Increasing tool-tip displacement corresponds to increasing power; the small numbers represent settings of the power control on the bonder. The error bars represent one sample standard deviation above and below the mean.)

made in each group to obtain one datum. The optimum force and time were found to be 30 gf (0.29 N) and 45 ms, respectively. Measured pull strengths of bonds made with these optimum bonding schedule parameters are given in figure 15 as a function of tool tip vibration amplitude. All bond loops broke or lifted off at the first bond. Also shown in the figure are the typical wire deformation in wire diameters (upper horizontal axis) and power supply dial setting (small numbers by each datum). The error bars represent one sample standard deviation above and below the mean.

From resolution of forces [1] the indicated pull strength is also the actual force in the wire at rupture. The bond efficiency, the ratio of pull strength to wire tensile strength, was greater than 65 percent, an unexpectedly high value, over a very wide range of ultrasonic power. Even at very large bond deformations the average pull strength of the gold wire was greater than 7 gf (0.07 N). This appears to be possible because of the metallurgical properties of gold. Aluminum is reported to work harden during ultrasonic welding [3] resulting in a damaged, brittle bond heel. While an aluminum wire bond with deformation of three wire diameters has an average pull strength of only about 3 gf (0.03 N), the thinned, widened heel of a gold wire bond appears to retain the normal strength of its remaining cross sectional area because there is little ultrasonic work damage. Such strength at high deformation is well known in thermocompression bonding, but in that case it has been generally assumed that the heat during bonding is sufficient to recrystallize the material as it is being deformed.

The above work involved only one type of gold wire. If the high strength, high deformation results are verified with other wire, this information should be taken into account in establishing visual inspection criteria.

(G. G. Harman and C. A. Main)

Plans: Preparation of a summary of the experimentally-measured effects and analysis of varying wire bond pull test parameters will be continued. Construction of a hot-melt glue puller for beam leads and optimization of bonding schedule for the beam lead bonding machine will be completed. Ribbon wire bonding studies on thick film, non-gold metallizations will be concluded. The wire bond puller will be modified for use with large diameter wire and the feasibility of adding real-time data resolution capability using a laboratory minicomputer will be investigated. Additional studies of the bonding characteristics of gold wire will be made on wire from different sources.

4.3. SCANNING ELECTRON MICROSCOPY

Objective: To evaluate scanning electron microscopy as an inspection, process control, or device characterization tool for use in the electron device industry with initial emphasis on evaluation of inspection procedures and development of methods suitable for industrial use.

Progress: Additional accessories to complement the basic functions of the scanning electron microscope (SEM) were installed. These include an eucentric stage for specimen manipulation and a micromanipulator by means of which a probe may be positioned and viewed in the specimen chamber. With a fine tipped tungsten probe mounted, the manipulator was used to apply a voltage to contact areas for voltage contrast studies. It was also used to break a wire bond of the type used in semiconductor devices. A video tape recording was successfully made of the breaking of the wire bond. (W. J. Keery)

Initial examinations of the various elements of a quadruple 2-input positive nand gate were made using the voltage contrast mode to observe the potentials of various elements of the circuit under the four possible input conditions.

(K. O. Leedy)

The literature is being searched to obtain references to device degradation, or changes in electrical characteristics, resulting from testing with an SEM.

(D. E. Sawyer)

Plans: A jig with suitable current-collecting electrodes will be designed and constructed to facilitate the examination of test structures and other devices in the

electron beam induced current (EBIC) mode. A flying spot scanner will be built for use in examining devices after exposure to the beam of the SEM. Compilation and review of reports of temporary or permanent changes in electrical characteristics of devices resulting from testing with an SEM will continue.

4.4. TEST PATTERN EVALUATION

Objective: To evaluate test patterns containing various test structures, such as MOS capacitors and p-n junctions, to develop and analyze new test pattern structures as appropriate, and to demonstrate how information obtained from test structures can be used to control fabrication processes.

Background: Special device configurations are widely used to monitor process procedures. These configurations are designed so that the measured electrical characteristics can be interpreted as directly as possible in terms of the desired process parameters. Patterns of these device structures may be included on each integrated circuit chip or they may be spotted at selected points on the wafer.

This task area was established to consolidate the work in the program on test structures of various kinds. The approach includes: (1) development, fabrication, and application of patterns for evaluating and controlling in-house processing of bipolar and MOS test devices; (2) collection and analysis of test structures developed and used elsewhere, and (3) eventual preparation of a test pattern catalog with identification of equivalent or nearly equivalent structures to aid in development of procurement specifications.

Initial work in this task area began last quarter. During that period, test pattern NBS-2, an array of 20 test structures, was designed and the mask set obtained (NBS Tech. Note 788, pp. 15-17).

Progress: The results of the first fabrication run on test pattern NBS-2 identified several problem areas in the in-house bipolar process. The boron nitride base diffusion was studied using the base sheet resistor test structure. Variations of resistivity over the entire slice as low as ±3.2 percent (two relative sample standard deviations) were observed.

Slice Evaluation — Test pattern NBS-2 (NBS Tech. Note 788, pp. 15-17) was completely fabricated including both the boron and phosphorus diffusions into both n-type bulk slices and n/n^+ epitaxial slices. This fabrication run is the first of a series intended to demonstrate the use of a test pattern in controlling process parameters. Electrical tests made at room temperature on the test slices after they were fully metallized revealed several problem areas. A summary of the results of

Table 5 — Measurements on Test Pattern NBS-2, Run No. 2.1

Test Structure[a]	Quantity Measured	Measured Value: Bulk (606)	Measured Value: Epitaxial (2105)	Target Value
14	Base Sheet Resistance, Ω/□	330	390	100±20
15	Emitter Sheet Resistance, Ω/□	160	140	10±5
16	Metal-to-Base Contact Resistance, $(\Omega\cdot mil^2)$[b]	3.5	3.2	<5
17	Metal-to-Emitter Contact Resistance, $(\Omega\cdot mil^2)$[b]	1100	2100	<5
18	Back-side Contact Resistance, Ω	190	1	<1
12	Fixed Oxide Charge Density, cm^{-3}	6.5×10^{11}	7.2×10^{11}	$(2.5\pm0.5)\times10^{11}$
12	Doping Density, cm^{-3}	4.3×10^{14}	4.9×10^{14}	—
12	Collector Oxide Thickness, Å	6400	6500	5000±500
6	Junction Bulk Leakage @ 5 V, nA/cm^2	28	3.7	<5
6	Surface Recombination Velocity, cm/s	85	—	<10

[a] See table 1 and figure 6, NBS Tech. Note 788, pp. 16-17 for identification of test structures.

[b] $1\ \Omega\cdot mil^2 \approx 645\ \Omega\cdot\mu m^2$.

selected measurements is listed in table 5 together with the desired target values. The data in the table indicate that the test pattern may be used over a wide range of values in addition to showing where the target values were missed.

In many cases the target values can be reached merely by zeroing-in certain aspects of the process. However, for certain quantities, fundamental process changes must be effected before they can be reached. The problem areas of this type identified by electrical tests on the test pattern were: (1) high metal-to-emitter contact resistance (structure 14); (2) high back-side contact resistance in bulk slices (structure 18); (3) high fixed oxide charge density (structure 12); and (4) excessive junction surface leakage (structure 6).

The high metal-to-emitter contact resistance appears to result from staining of the boron-diffused regions prior to phosphorus deposition. Steps to eliminate this problem are under study. The high back-side contact resistance in bulk slices was due

to a gold compensated layer formed during the alloying of the contact; use of antimony-doped gold is expected to eliminate this problem. The high fixed-charge density appears to be caused by a final oxidization which ended in an oxygen ambient; the process was changed so that all oxidizations now end in a nitrogen ambient which is expected to eliminate this problem. Excessive junction surface leakage, manifested by high surface recombination velocity, appears to be caused by both generation currents from interface states and tunnel current. A proper annealing step after the aluminum metallization is expected to cure the interface state problem, and use of a lower base surface concentration is expected to reduce the tunnel current.

Base Sheet Resistance Study — In the production of high yield electronic components it is essential to have tight control over various processing steps. In the production of bipolar components the base diffusion is a critical step. The variation of the base diffusion from a boron nitride source as a function of position in the diffusion boat or as a function of location on a 1.5-in. diameter wafer (38-mm) was studied using an array of sheet resistor test structures. In addition the results of measurements on the test structure array were compared with results of four-probe sheet resistance measurements.

Eight silicon slices were first oxidized. Six slices were patterned with the base diffusion mask of test pattern NBS-2 using standard photolithographic procedures. Two slices were stripped completely of oxide to provide pilot slices for the four-probe measurements. The slices were arranged in the diffusion boat with five boron nitride source slices in the order listed in table 6 with a spacing of 67 mils (1.7 mm) between slices. The patterned or stripped side of each silicon slice faced its neighboring boron nitride slice during predeposition diffusion at 1000°C for 15 min in dry oxygen followed by dry nitrogen. The slices were then removed from the furnace and deglazed in 10 percent hydrofluoric acid solution for 30 s and then rinsed and dried. Finally they were diffused at 1000°C for 20 min in dry oxygen, followed by 30 min in wet oxygen, followed by 20 min in dry nitrogen. This process led to a sheet resistance of about 180 Ω/□ and a junction depth of about 1.1 μm.

Sheet resistance was measured by the four-probe method [1] on pilot slices and with the sheet resistor test structure on patterned slices. The base sheet resistor test structure in test pattern NBS-2 is shown in figure 16. In operation a 1-mA current, I, is passed between the outer contacts and the voltage difference, ΔV, is measured between the inner pair of contacts. The current is reversed to check for linearity; on reversal of I, ΔV remained constant, in all cases, to well within 0.5 percent. The geometry of this structure conforms to the ASTM standard [2] for such a pattern. In the art work sent to the mask manufacturer the region between the voltage contacts was specified to be 3 squares wide by 11 squares long, a ratio of

Table 6 — Base Sheet Resistance Values, Run No. 2.2

Slice	Kind	Sheet Resistance, Ω/□
Boron Nitride		
Silicon No. 1	Pilot	192±23
Silicon No. 3	Patterned	182±6
Boron Nitride		
Silicon No. 4	Patterned	179±8
Silicon No. 2	Pilot	181±12
Boron Nitride		
Silicon No. 5	Patterned	174±11
Silicon No. 6	Patterned	182±6
Boron Nitride		
Silicon No. 7	Patterned	183±14
Silicon No. 8	Patterned	192±21
Boron Nitride		

0.273. This geometrical factor was measured photographically to be 0.290±0.001. The uncertainty of ±0.3 percent arises from slice-to-slice variation; variations on a slice could not be detected. Using the experimentally determined value for the geometrical factor, the base sheet resistance was computed as $R_s = 0.290 \times \Delta V/I$ where R_s has units of ohms per square (Ω/□) if ΔV is in millivolts and I is in milliamperes.

The base sheet resistance map for slice number 6 is shown in figure 17. The mean sheet resistance was 182 Ω/□; the sample standard deviation was 3 Ω/□. Similar measurements were made on the other slices. The results are shown in the last column of table 6 in which the mean value ± two sample standard deviations is listed for each slice. These results indicate that slices on either end of the diffusion boat have a higher sheet resistance and more dispersion in values than those in the middle of the boat. This suggests that these slices (Nos. 1 and 8) were cooler during the diffusions. The uniformity of the other slices is satisfactory for test purposes. Sheet resistance values measured on the test pattern agree within experimental error with those measured by the four-probe method on the pilot slices diffused at the same time.

(M. G. Buehler, T. F. Leedy, R. L. Mattis, F. R. Kelly, and J. Krawczyk)

Plans: Collection and analysis of test structures used in the industry will begin. Additional fabrication runs of test pattern NBS-2 will be made to further the development of both bipolar and MOS processes.

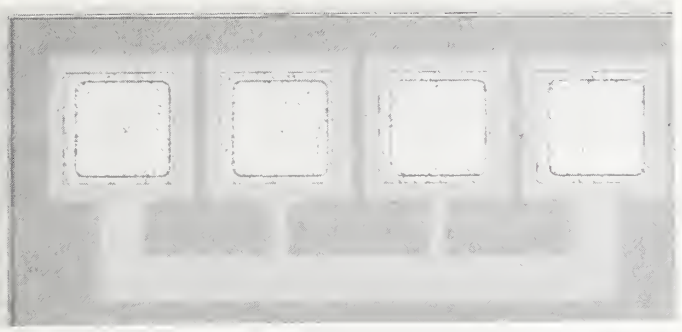


Figure 16. Base sheet resistor test structure. (The center-to-center spacing between bonding pads is 11 mils (0.28 mm).)

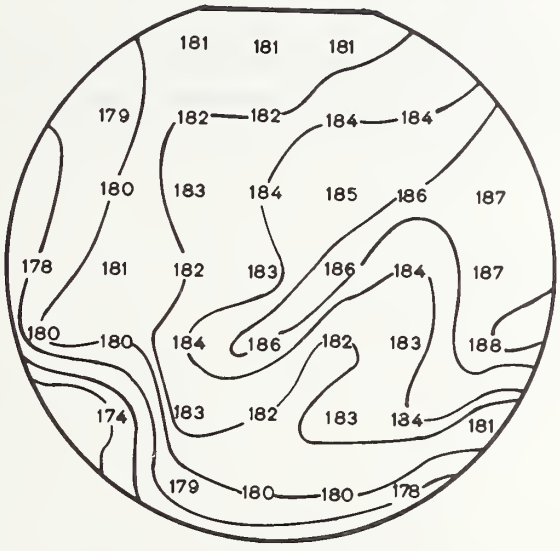


Figure 17. Base sheet resistance variations across Slice No. 6, Run 2.2.

4.5. REFERENCES

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2. Reference 1, p. 9.

4.2. Interconnection Bond Evaluation

1. Schafft, H. A., Testing and Fabrication of Wire-Bond Electrical Connections — A Comprehensive Survey, NBS Technical Note 726 (September, 1972), pp. 61-66.

2. Reference 1, p. 66, eqs (5.3.10) and (5.3.11).

3. Coucoulas, A., Ultrasonic Welding of Aluminum Leads to Tantalum Thin Films, *Trans. Met. Soc. of AIME* 236, 587-589 (1966).

4.4. Test Pattern Evaluation

1. Standard Method for Measuring Resistivity of Silicon Slices with a Collinear Four-Probe Array, ASTM Designation F84-72, *Annual Book of ASTM Standards*, Part 8. Available as a separate reprint from American Society for Testing and Materials, 1916 Race Street, Philadelphia, Pa. 19103.

2. Standard Method for Measuring Hall Mobility and Hall Coefficient in Extrinsic Semiconductor Single Crystals, ASTM Designation F76-72, *Annual Book of ASTM Standards*, Part 8. Available as a separate reprint from American Society for Testing and Materials, 1916 Race Street, Philadelphia, Pa. 19103.

5. SEMICONDUCTOR DEVICES

5.1. THERMAL PROPERTIES OF DEVICES

Objective: To evaluate and improve electrical measurement techniques for determining the thermal characteristics of semiconductor devices.

Progress: A summary of the results of the preliminary round-robin experiment on thermal resistance being conducted in cooperation with EIA-JEDEC Committee JC-25 on Power Transistors confirmed the previously reported results that the V_{CB} technique gives lower values of thermal resistance than the V_{BE} base-and-collector switching technique (NBS Tech. Note 717, pp. 31-32) and that the latter gives lower values than the V_{EB} emitter-only switching technique (NBS Tech. Note 702, pp. 23-25).

A study was undertaken to determine whether the measurement of d-c current gain, h_{FE}, as a function of collector-emitter voltage, V_{CE}, for constant collector current and case temperature can be used as a screen to predict accurately when the electrical measurement of thermal resistance deviates significantly from the thermal resistance as derived from the measurement of peak junction temperature. It had been observed previously that in cases where the change in h_{FE} is abrupt, the deviation occurs at a value of V_{CE} very close to that at which h_{FE} changes abruptly. For less abrupt changes in h_{FE}, it was found that significant deviations may occur at voltages below that at which h_{FE} is a maximum; hence, in such cases the h_{FE} screen may not be an accurate predictor.

A preliminary study was undertaken to determine the optimum extrapolation procedure for semiconductor device thermal resistance measurements. Initial results indicate that a log-linear extrapolation procedure is appropriate for use for the first few hundred microseconds of cooling on devices that can be approximated by a round silicon chip on an infinite heat sink. Some signal and rectifier diodes and thyristors fall into this category.

Standardization Activities — Analysis of the results of the preliminary round-robin experiment on thermal resistance being conducted in cooperation with EIA-JEDEC Committee JC-25 on Power Transistors was completed. Data usable for comparison purposes were obtained from four of the seven participants. In all, three techniques for measuring thermal resistance were compared. Two laboratories reported values measured according to the V_{BE} base-and-collector switching technique, and four reported values measured according to the V_{CB} emitter-and-collector switching technique. In addition, measurements were made at NBS by the V_{EB} emitter-only switching technique, which is the proposed referee method for measuring thermal resistance of power transistors.

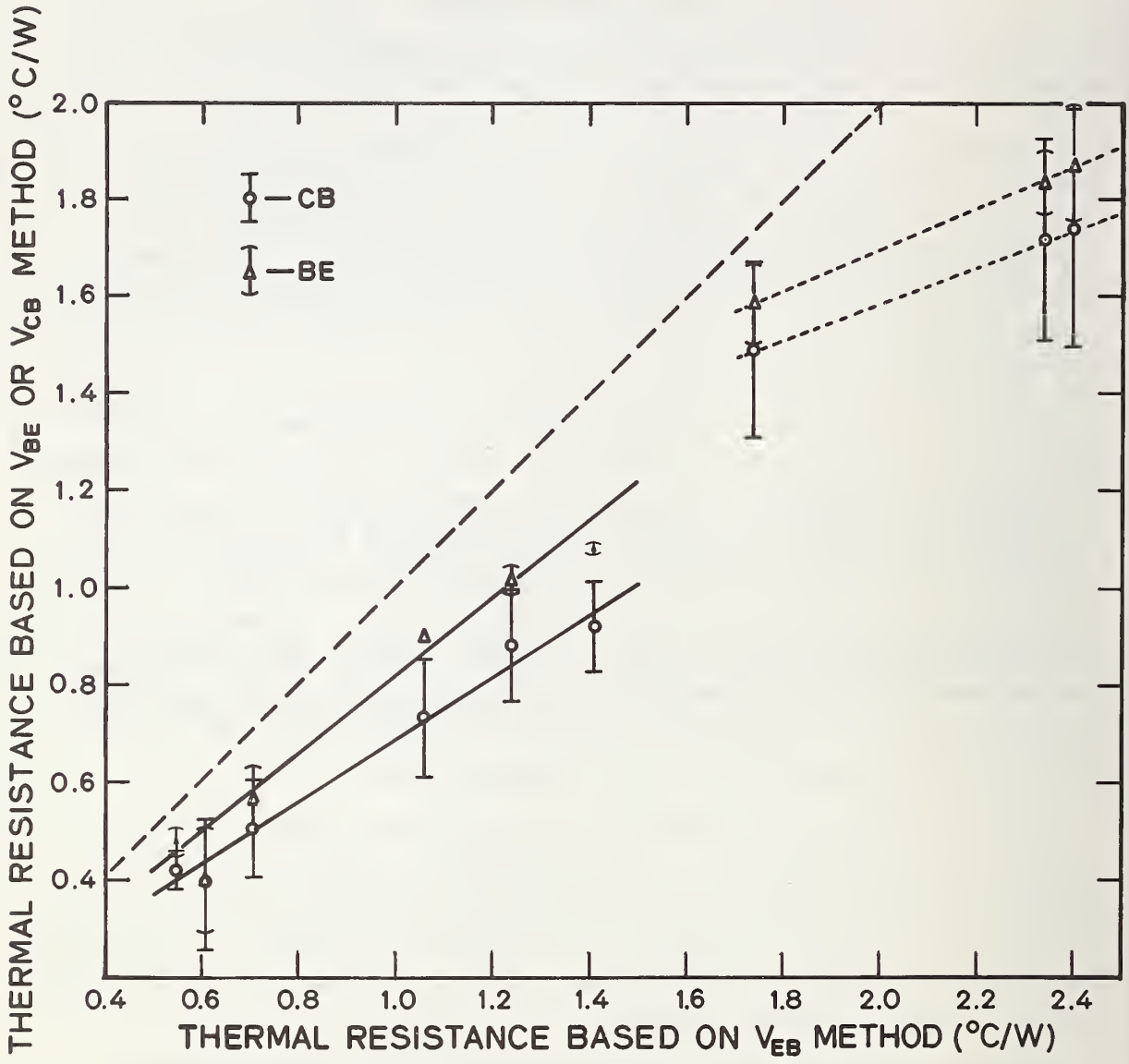


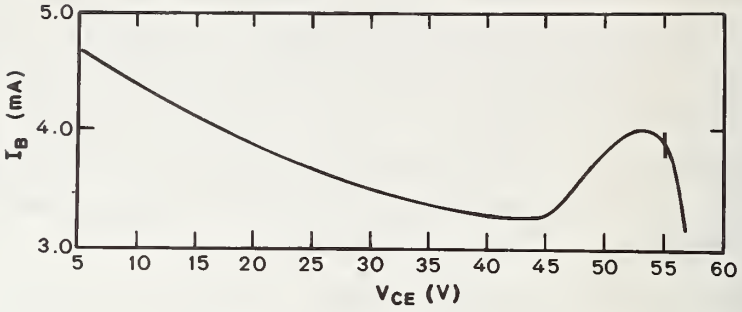
Figure 18. Thermal resistance of power transistors. (Data are shown for transistors in TO-3 and TO-66 cans, solid and dotted lines, respectively. The dashed line is the value that would be measured if all methods gave the same result.)

Ten devices were measured. Three were encased in TO-66 cans and seven in TO-3 cans. The average value of thermal resistance of each device, for both the V_{CB} and V_{BE} techniques, is plotted in figure 18 against the value of thermal resistance as measured using the V_{EB} emitter-only switching technique. The error bars represent one sample standard deviation above and below the mean. As expected, the V_{CB} technique gave lower values of thermal resistance than the V_{BE} base-and-collector switching technique, which in turn, was lower than the V_{EB} emitter-only switching technique. It can be seen that the TO-3 and TO-66 encased devices form two distinct classes.

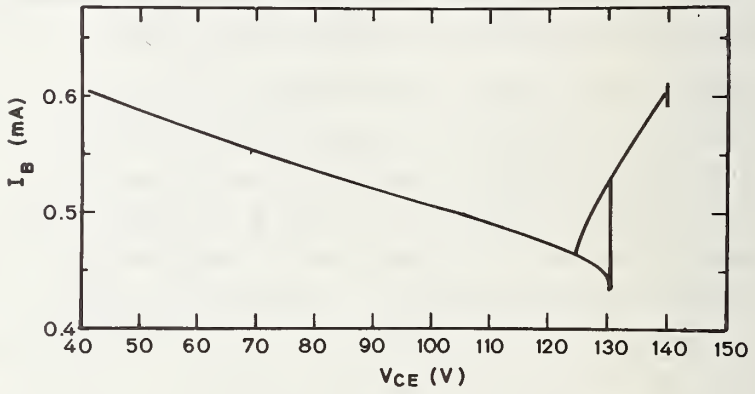
Draft copies of proposed thermal resistance test methods for signal diodes and power transistors were completed and circulated to JEDEC Committees JC-20 on Signal and Regulator Diodes and JC-25 on Power Transistors, respectively, for review prior to submission as an official committee letter ballot. (F. F. Oettinger)

Screen for Hot Spots — Further studies were performed to determine whether the measurement of d-c current gain, h_{FE}, as a function of collector-emitter voltage, V_{CE}, for constant collector current and case temperature can be used to predict when the electrical measurement of thermal resistance deviates significantly from the thermal resistance as derived from the measurement of peak temperature made with the infrared microradiometer. Measurements of h_{FE} as a function of V_{CE} were made on a group of devices with the same low collector current as was used previously in measuring thermal resistance (NBS Tech. Note 788, p. 49 and table 6). The results on three devices which previously showed indications of severe current crowding through deviations between electrical and infrared measurements of thermal resistance are presented in figure 19 in the form of curves of base current as a function of V_{CE} for constant collector current. The results confirm that severe current crowding should occur in each of these devices under the conditions of the thermal resistance measurement. In the case of device No. 1, the thermal resistance was measured under conditions approaching avalanche breakdown. In the case of device No. 4, the thermal resistance was measured above the abrupt change in h_{FE}; previously (NBS Tech. Note 571, pp. 35-41) it has been shown that the deviation between electrical and infrared measurements of thermal resistance increases abruptly at the same value of V_{CE} as that at which the abrupt change in h_{FE} occurs. In the case of device No. 10, the thermal resistance was also measured above the minimum in I_B; additional measurements of thermal resistance at V_{CE} = 40 and 45 V also showed significant discrepancies between the electrical and infrared results. In this case, therefore, the h_{FE} measurement cannot be used to predict the exact value of V_{CE} at which the hot spot occurs and where deviations between electrical and infrared measurements of thermal resistance may be expected. Measurements of h_{FE} on

a. Device No. 1
I_C = 400 mA
T_C = 25°C



b. Device No. 4
I_C = 100 mA
T_C = 25°C



c. Device No. 10
I_C = 400 mA
T_C = 25°C

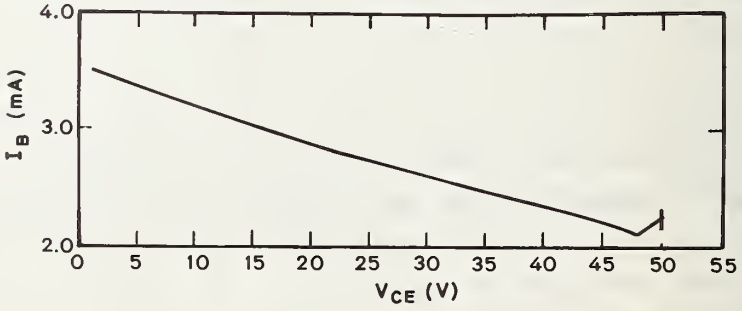


Figure 19. Base current, I_B, as a function of collector-emitter voltage, V_{CE}, for three transistors which exhibit severe current crowding. (Base current is inversely proportional to common emitter current gain under the conditions of the measurement. Thermal resistance was measured previously by both electrical and infrared techniques at the value of V_{CE} indicated by the vertical bar.)

the other devices in the group, for which the electrical and infrared measurements of thermal resistance agreed to within 20 percent, showed in all cases no evidence of abrupt changes in h_{FE} at voltages up to that used for the thermal resistance measurements. (S. Rubin, D. L. Blackburn, and F. F. Oettinger)

Thermal Resistance Methods — The TRUMP [1] computer program was used to investigate various extrapolation procedures for use in determining thermal resistance. An extrapolation procedure is needed because significant cooling occurs during the delay time before the temperature sensitive parameter can be measured after the heating pulse is terminated. The structure studied was a cylindrical silicon chip, 0.288 cm in diameter, on an infinite heat sink with the heat source on the top surface.

If it is assumed that during the first few hundred microseconds of heating, the change in temperature in the plane of the heat source, $\Delta T_{JR}(t)$, can be represented by [2]:

$$\Delta T_{JR}(t) = 1.1\ P\sqrt{t}/(A\sqrt{k\rho c}), \tag{6}$$

where P is the power applied in the plane of the heat source in watts, t is the time following application of power in seconds, A is the chip cross sectional area (0.065 cm^2), k is the thermal conductivity (0.90 $W/cm\cdot{}^{\circ}C$), ρ is the mass density (0.71 g/cm^3), and c is the specific heat (2.33 $W\cdot s/g\cdot{}^{\circ}C$), and that the cooling curve is the conjugate of the heating curve once the steady state temperature is reached [3], the temperature in the plane of the heat source, T_J, is given by:

$$T_J = T_R + (PL/kA) - \Delta T_{JR}(t) \tag{7}$$

where T_R is the temperature of the heat sink in degrees Celsius, L is the chip thickness (0.0259 cm), and t is now the time after the termination of power in seconds.

The steady-state temperature computed by the TRUMP program for an applied power of 100 W was 44.23°C above the heat sink temperature. This compares favorably with 44.18°C calculated from eq (7) for t = 0. During the first 200 μs of cooling the maximum difference between the temperature computed by TRUMP and the temperature calculated from eq (7) occurred at t = 200 μs; here the temperature computed by TRUMP was 0.55°C below the value (24.64°C above the heat sink temperature) calculated from eq (7).

The TRUMP program was also used to compute the peak surface temperature during the first 200 μs of cooling for a silicon chip with circular heat source areas 42 and 22 percent of the chip surface area. In addition, the average surface

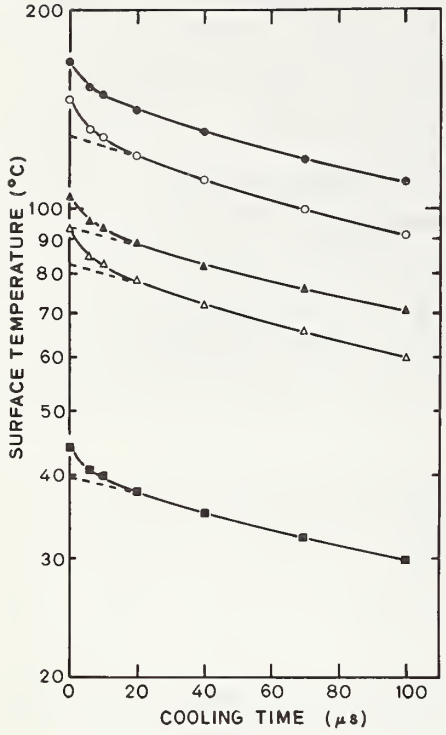


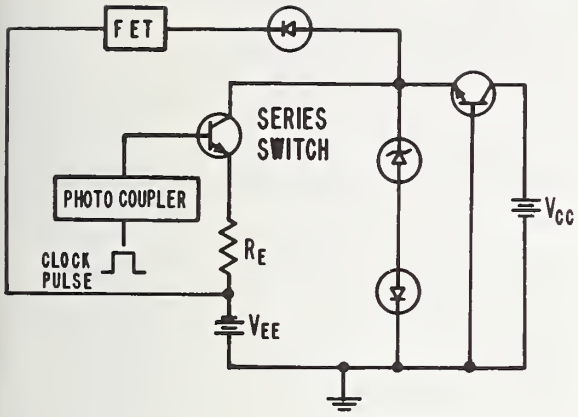
Figure 20. Computed peak (solid points) and average (open points) surface temperature as a function of cooling time for a round silicon chip on an infinite heat sink with a power dissipation of 100 W in several different heat source areas expressed as a percentage of the total chip area. (Heat source area: 22% - ●, ○; 42% - ▲, △; 100% - ■)

temperature of the heat source area, T_{JAVG}, was computed from the TRUMP results and the relationship (NBS Tech. Note 727, pp. 47-48):

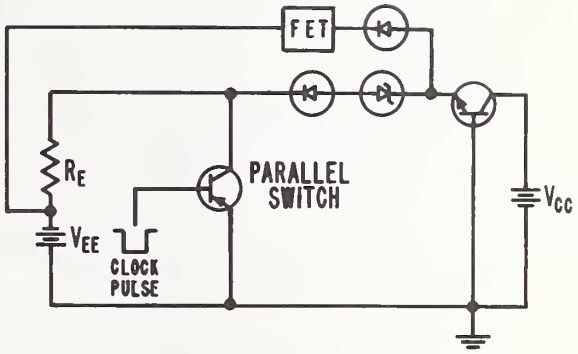
$$T_{JAVG} = \frac{\sum_i T_i A_i}{\sum_i A_i}$$

where T_i and A_i are the temperature and area respectively of the i^{th} element.

The results of the TRUMP computations were plotted in a variety of ways to find the most linear representation. This was obtained by plotting the logarithm of temperature as a function of time as shown in figure 20 for the first 100 μs of cooling. For the case where the entire chip surface is the heat source (100% curve) the average and peak surface temperatures are identical. The cooling curves are approximately straight and parallel during the interval between 20 and 100 μs. If these straight regions are extrapolated back to t = 0 as indicated by the dashed lines in the figure, values obtained are about 10 percent lower than the computed value. When the peak temperature is different from the average temperature, which



a. Series switching



b. Parallel switching

Figure 21. Circuits for measuring thermal resistance by the emitter-only switching technique.

is usually the quantity determined in electrical measurement of thermal resistance, the extrapolated values of average temperature are between 20 and 25 percent lower than the computed peak temperature at t = 0 for the same heat source area.

It should be emphasized that in this initial study the thermal conductivity for the silicon chip was assumed to be independent of temperature. In addition, it should be noted that only a few devices have geometry appropriate to the model proposed. Some signal and rectifier diodes and some thyristors meet the assumptions of the model. (F. F. Oettinger and R. L. Gladhill)

Long term single-operator measurements were undertaken to check the repeatability of the equipment for measuring thermal resistance of transistors by the emitter-only switching technique. During a 7-week period, 11 to 15 sets of measurements were made on seven test devices. Two devices (lot A) were single diffused transistors in TO-66 cans, two devices (lot NM) were epitaxial transistors in TO-66 cans, and three devices (lot AA) were single diffused transistors in TO-3 cans.

The test conditions were chosen to provide sufficient power dissipation to ensure a reasonable rise in junction temperature but not enough power or voltage to cause significant current crowding. Heating current was 1 A for the devices in TO-66 cans (Lots NM and A) and 2 A for the devices in TO-3 cans (Lot AA). In both cases the collector-emitter voltage was 20 V. A measuring current, I_m, of 6 or 12 mA was used.

Table 7 — Pooled Results of Thermal Resistance Repeatability Experiment

	Thermal Resistance, °C/W	
	I_m = 6 mA	I_m = 12 mA
Lot NM; Case Temperature, 25°C		
Parallel Switching	5.57±0.03	5.56±0.03
Series Switching	5.59±0.03	5.58±0.03
Lot A; Case Temperature, 25°C		
Parallel Switching	2.53±0.03	2.52±0.02
Series Switching	2.54±0.04	2.52±0.03
Lot AA; Case Temperature, 25°C		
Parallel Switching	0.75±0.01	0.75±0.01
Series Switching	0.75±0.01	0.75±0.01
Lot AA; Case Temperature, 60°C		
Parallel Switching	0.78±0.01	0.78±0.01
Series Switching	0.78±0.01	0.78±0.01

The temperature sensitive parameter was measured 5, 10, 50, and 100 μs after the heating power pulse was terminated. Measurements were made with both circuits shown in figure 21 in order to compare the series-switching and parallel-switching techniques. These circuits also incorporate an FET constant-current regulator to provide the measuring current from the zener-diode-regulated V_{EE} supply. The diode in series with the FET regulator protects the regulator from damage due to a high reverse voltage from the emitter heating supply when the emitter lead is opened while the emitter supply is connected.

The case temperature was measured using the washer technique (NBS Tech. Note 555, pp. 44-45) in which a thermocouple is embedded in nickel-plated copper washer at a location underneath the chip approximately 50 μm below the case-washer interface. All devices were tested with a case temperature of 25°C while the TO-3 encased devices were also tested with a case temperature of 60°C.

The results of the measurements obtained for a delay time of 10 μs for the lot NM and AA devices and 20 μs for the lot A devices are listed in table 7. Since more than one device of each type was measured, the results for the individual device types are pooled. The results indicate that the degree of agreement between the series and parallel switching techniques as well as for the two measuring currents used is quite acceptable. Since the parallel switching technique requires a less complicated circuit, it would be preferred in most practical situations.

The data also indicate that for the TO-66 encased devices, the sample standard deviation was nearly constant even though the thermal resistance varied from 2.5 to 5.6°C/W. For the TO-3 encased devices, even though the thermal resistance was

measured at case temperatures of 25 and 60°C, the sample standard deviation was also constant. If the measured thermal resistance is multiplied by the heating power, the sample standard deviation of the resulting junction-to-case temperature difference ranges from 0.4 to 0.6°C for the parallel emitter switching technique. Thus, these initial measurements confirm that the repeatability is nearly independent of the magnitude of the measured thermal resistance, but is limited by a minimum resolvable junction-to-case temperature difference.

During this series of measurements, it was found that the temperature sensitive parameter, V_{EB}, at zero power and 25°C did not return to its original value following measurements over the temperature range 25 to 100°C. However, if the retaining screws were loosened and the transistor moved about on the heat sink and the retaining screws retightened, then V_{EB} returned to, or much closer to, its initial 25°C reading. This appears to indicate that the silicone grease, which is a component of the material used as a thermal interface between the case and heat sink, runs at 100°C and changes the thermal characteristics of the interface. This potential source of variation can be minimized by making the measurements in the following order. First, make the measurements of V_{EB} necessary to determine the change in the temperature sensitive parameter due to the dissipation of power. For these measurements the case temperature is kept at a constant preset value. After this is complete, generate the calibration curve by measuring the temperature sensitive parameter as a function of case temperature starting at the lowest case temperature of interest. Because the calibration curve is generated with very low power dissipation in the device, variations in the thermal characteristics of the interface do not affect the result. (S. Rubin and F. F. Oettinger)

Plans: The results of the preliminary round-robin experiment on thermal resistance measurements being conducted in cooperation with JEDEC Committee JC-25 on Power Transistors will be compared with thermal resistance derived from measurements of peak junction temperature to be made with the infrared microradiometer. Work on the JEDEC committee letter ballots on proposed thermal resistance test methods for signal diodes, power transistors, and integrated circuits will be undertaken.

Further studies will be performed to compare measurements of thermal resistance using the emitter-only switching technique with that of the thermal resistance derived from measurements of peak junction temperature made with the infrared microradiometer under conditions such that the device under test will be operating at junction temperatures at or near 80 percent of its rated maximum junction temperature. The twelve transistors measured this quarter will be used in this study.

The investigation of extrapolation procedures for use in determining thermal resistance will be continued. Such effects as the change in silicon thermal

conductivity with temperature will be taken into account in the thermal analysis calculations.

Long-term, single-operator measurements, to check the repeatability of the equipment for measuring thermal resistance of transistors by the emitter-only switching technique, will be continued. The measurements will be made on TO-3 encased transistors using parallel-emitter switching at a case temperature of 60°C.

5.2. MICROWAVE DEVICE MEASUREMENTS

Objective: To study the problems and uncertainties associated with the measurement of electrical properties of microwave diodes, and to improve the techniques of these measurements.

Progress: The mixer conversion loss repeatability studies were continued using a Schottky-barrier diode. This diode was found to be sensitive to mechanical shock, as were the point-contact types used previously. In the standards area, a limited revision was made of the IEC standard on microwave mixer measurements, and mixer terminology that appears to be acceptable to both the IEEE and EIA was prepared in collaboration with members of the latter.

Repeatability Studies — The sample standard deviations for each day's conversion loss measurements have ranged between 0.027 dB and 0.036 dB. As with previous measurements (NBS Tech. Note 788, pp. 51-52), the data were taken in groups, each group being formed by repeated cycling of the modulation attenuator. An odd number of cycles was used, varying between three and eleven, allowing easy selection of the group median. For three or more data per group, the sample standard deviations of the group medians ranges between 0.010 dB and 0.033 dB; only one of 14 groups exceeded 0.024 dB. For only the first cycle in each group, the sample standard deviations ranged between 0.022 dB and 0.055 dB; four of six groups exceeded 0.024 dB.

Most of the sample standard deviations were appreciably larger than the 0.015 dB standard deviation estimated from the calorimeter voltage increment measurements. The differences in the medians or the means from one day to another were even larger; the maximum differences ranged from 0.098 to 0.113 dB depending upon which median or mean was used. This drift was also observed during lengthy runs; the second half of the data consistently appeared to have drifted slightly with respect to the first half. The ambient temperature was recorded for all measurement groups, but never varied more than 0.1 or 0.2°C; these variations did not seem to correlate with conversion loss variations.

The day-to-day drift (and perhaps some of the within-day variations) may be explained by the sensitivity to mechanical shock of the Schottky-barrier diode used for these measurements. It had been expected that the Schottky diodes would be relatively insensitive to mechanical shock, and it was for this reason that they were used instead of the highly shock-sensitive point-contact types. It was discovered, however, that rotating a waveguide switch audibly against its stop was sufficient to change the output voltage of one type of Schottky diode. The shock sensitivity of a Schottky diode obtained from a different supplier seemed to be much less, although not completely eliminated.

Seven mounted compensated thermistor type bolometers were recalibrated.* Measurements were started to intercompare these bolometers and to re-establis- the proper monitor-calorimeter voltage to use for maintaining exactly 1 mW of local oscillator power available to the mixer. These initial measurements indicate appreciable differences between bolometers; some bolometers cannot be used at their rated balance resistance with the manual power bridge due to inadequate matching of their elements.

Standardization Activities — A partial revision of IEC Document 47 (Central Office) 376 on Microwave Mixer Measurement Methods was completed at the request of the U. S. National Committee (USNC). A complete revision was made of the section on overall average noise figure, and the i-f average noise figure subtraction method for measuring output noise ratio was substituted for an unworkable method. A number of other recomendations were made, but the changes were limited to those endorsed by the USNC.

Mixer terminology was discussed with members of JEDEC Committees JC-10 on Terms and Definitions and JC-24 on Low-Power Transistors at a meeting of the former in Washington. Terms, definitions, and symbols were arrived at which were in reasonable agreement with the tentative terminology that had been formulated by the mixer and detector task group of the Standards Committee of IEEE Group on Electron Devices. (J. M. Kenney)

Plans: Further power measurements will be made in an attempt to resolve the differences between bolometers and establish the proper monitor-calorimeter voltage. Work will then be resumed on the conversion loss random uncertainty determination.

*These calibrations were performed by M. Weidman of the NBS Electromagnetics Division.

5.3. CARRIER TRANSPORT IN JUNCTION DEVICES

Objective: To improve methods of measurement for charge carrier transport and related properties of junction semiconductor devices.

Progress: Measurements were made with the Sandia bridge on a 2N2907A silicon *p-n-p* transistor after gain degradation by neutron irradiation. The results showed that the large variations in delay time then measured could be reduced significantly by applying the appropriate correction factor. However, unlike the case of a 2N2219 *n-p-n* silicon transistor previously reported, a significant increase in delay time was observed.

In the S-parameter round robin, the between-laboratory variability for transistor measurements was compared with the between-laboratory variability of the measurements on the R-C networks made under the same conditions and found to be within the expected range, indicating that there is no basis for concluding that additional variability is introduced in the transistor measurements.

Sandia Bridge Delay-Time Instrumentation — Measurements were made on a 2N2907A *p-n-p* silicon transistor under conditions almost identical to those used previously for measurements on a 2N2219 *n-p-n* silicon transistor (NBS Tech. Note 788, pp. 53-55); the collector-base voltage was 2 V, rather than 5 V as in the previous measurements. Both transistors were irradiated at the same time and at the same fluence. Before irradiation, the value of the small signal, common-emitter current gain, h_{fe}, at a collector current of 20 mA for the 2N2907A was about 160, and after irradiation it was about 8.

Figure 22 is a plot of the delay time measured before irradiation, curve A; the delay time measured after irradiation, curve B; and the delay time corrected as previously described for the effects of extraneous pickup, curve C. The large variation in delay time from 3 to 7 MHz following irradiation is reduced but not eliminated by the addition of the correction term. Unlike the previous results for the 2N2219, the initial and corrected delay times are quite different. The average corrected delay time is about 21.5 percent larger than 762 ps, the average value of the delay time before irradiation. (D. E. Sawyer)

Interlaboratory Comparison of S-Parameter Measurements — Transistor S-parameter measurements made in the interlaboratory comparison (NBS Tech. Notes 743, pp. 42-43 and 773, pp. 34-36) exhibited the same trends as those on passive devices (NBS Tech. Note 788, pp. 55-57). Since the transistors were measured only once at each bias by each laboratory, only the between-laboratory variability of these measurements could be determined. This variability was compared with the between-laboratory variability of the measurements on the R-C networks made under the same

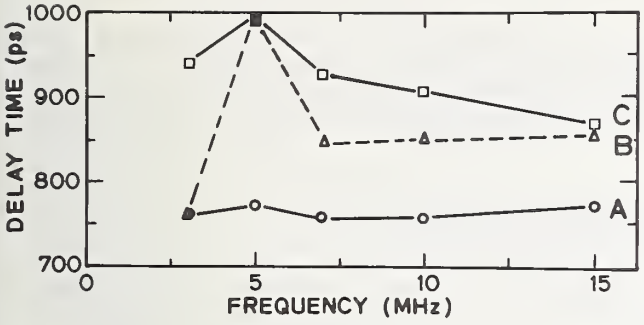


Figure 22. Delay time of a 2N2907A transistor before and after h_{fe} degradation. (A, before degradation; B, after degradation (measured); C, after degradation (corrected).)

conditions and found to be within the same range, indicating that there is no basis for concluding that additional variability is introduced in the transistor measurements. The method of setting transistor biases and the precautions taken to monitor changes in transistor characteristics were apparently sufficient to minimize differences caused by these factors.

As in the case of the R-C networks, the variability of the transistor reflection parameter measurements was greater than that for the transmission parameters. Data on the 2N3960 transistors were typical. Typically the coefficient of variation of the measurements of the magnitude of S_{12} and S_{21} was 5 percent or less, and the standard deviation of the phase measurements was a maximum of 1 deg. The coefficient of variation of measurements of the magnitude of S_{11} was as high as 15 percent in some cases and the standard deviation of the phase measurements was as large as 2.5 deg. The variability of the measurements of S_{22} was slightly less.

The variability of transistor S-parameter measurements could be decreased by specifying the calibration method to be used when the transistor fixture is employed. None of the calibration methods used by the participants (NBS Tech. Note 773, p. 35) completely compensated for the effects of the transistor fixture, and none had a clear advantage in this respect. Selecting one of them would reduce a major source of between-laboratory variability when the transistor fixure is used. Since only one of the participants had a 50-Ω termination for the transistor socket and since these terminations cannot be obtained easily, one of the other calibration methods should be selected. (G. J. Rogers)

Plans: Analysis of the results of the interlaboratory comparison of transistor scattering parameter measurements will be completed and a final report will be prepared. No further laboratory work in this task area is planned.

5.4. REFERENCES

5.1. Thermal Properties of Devices

1. Edwards, A. L., TRUMP: A Computer Program for Transient and Steady-State Temperature Distributions in Multidimensional Systems, Lawrence Radiation Laboratory, Univ. of California, Livermore, California, UCRL-14754, Rev. II, 1 July 1969. Available from the National Technical Information Service, Springfield, Virginia 22151.

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3. Gutzwiller, R. W. and Sylvan, T. P., Power Semiconductor Ratings Under Transient and Intermittent Loads, *AIEE Transactions, Part I, Communications and Electronics* 80, 699-706 (January, 1961).

APPENDIX A
JOINT PROGRAM STAFF

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APPENDIX B
COMMITTEE ACTIVITIES

ASTM Committee F-1 on Electronics

W. M. Bullis, Editor, Subcommittee 4, Semiconductor Crystals; Secretary, Subcommittee 91, Editorial; Leaks, Resistivity, Mobility, Dielectrics, and Compound Semiconductors Sections; Subcommittee 11, Quality and Hardness Assurance; Advisory Committee

J. R. Ehrstein, Chairman, Resistivity Section; Epitaxial Resistivity, and Epitaxial Thickness Sections

J. C. French, Chairman, Subcommittee 91, Editorial; Subcommittee 11, Quality and Hardness Assurance; Secretary, Advisory Committee

G. G. Harman, Secretary, Interconnection Bonding Section

B. S. Hope, Committee Assistant Secretary

K. O. Leedy, Chairman, Interconnection Bonding Section

T. F. Leedy, Photoresist and Dielectrics Sections

D. C. Lewis, Subcommittee 11, Quality and Hardness Assurance

C. P. Marsden, Committee Secretary; Advisory Committee

R. L. Mattis, Lifetime Section, Editorial Subcommittee

W. E. Phillips, Chairman, Lifetime Section; Secretary, Subcommittee 4, Semiconductor Crystals, Crystal Perfection, Mechanical Properties of Semiconductor Surfaces, Compound Semiconductors; Impurities in Semiconductors, and Germanium Sections

A. H. Sher, Germanium Section

W. R. Thurber, Mobility, Germanium, Compound Semiconductors, and Impurities in Semiconductors Sections

ASTM Committee E-10 on Radioisotopes and Radiation Effects

W. M. Bullis, Subcommittee 7, Radiation Effects on Electronic Materials

J. C. French, Subcommittee 7, Radiation Effects on Electronic Materials

Electronic Industries Association: Solid State Products Division, Joint Electron Device Engineering Council (JEDEC)

J. M. Kenney, Microwave Diode Measurements, Committee JC-21 on UHF and Microwave Diodes

F. F. Oettinger, Chairman, Task Group JC-11.3-1 on Thermal Considerations for Microelectronic Devices, Committee JC-11 on Mechanical Standardization; Technical Advisor, Thermal Resistance Measurements, Committees JC-22 on Rectifier Diodes and Thyristors, JC-20 on Signal and Regulator Diodes, JC-25 on Power Transistors, and JC-30 on Hybrid Integrated Circuits

S. Rubin, Chairman, Council Task Group on Galvanomagnetic Devices

D. E. Sawyer, Task Group JC-24-5 on Transistor Scattering Parameter Measurement Standard, Committee JC-24 on Low Power Transistors

H. A. Schafft, Technical Advisor, Second Breakdown and Related Specifications Committee JC-25 on Power Transistors

IEEE Electron Devices Group:

J. C. French, Standards Committee

J. M. Kenney, Chairman, Standards Committee Task Force on Microwave Solid-State Devices II (Mixer and Video Detector Diodes)

H. A. Schafft, Chairman, Standards Committee Task Force on Second Breakdown Measurement Standards

IEEE Magnetics Group

S. Rubin, Chairman, Galvanomagnetic Standards Subcommittee

IEEE Parts, Hybrids, and Packaging Group

W. M. Bullis, New Technology Subcommittee, Technical Committee on Hybrid Microelectronics

Society of Automotive Engineers

J. C. French, Subcommittee A-2N on Radiation Hardness and Nuclear Survivability

W. M. Bullis, Planning Subcommittee of Committee H on Electronic Materials and Processes

F. F. Oettinger, Electronic Systems Steering Committee

IEC TC47, Semiconductor Devices and Integrated Circuits:

S. Rubin, Technical Expert, Galvanomagnetic Devices; U.S. Specialist for Working Group 5 on Hall Devices and Magnetoresistive Devices

APPENDIX C

SOLID-STATE TECHNOLOGY & FABRICATION SERVICES

Technical services in areas of competence are provided to other NBS activities and other government agencies as they are requested. Usually these are short-term, specialized services that cannot be obtained through normal commercial channels. Such services provided during the last quarter are listed below and indicate the kinds of technology available to the program.

1. Thin Metal Films (J. Krawczyk)

Thin aluminum films were evaporated over tantalum-nitride-patterned glass substrates for the NBS Dimensional Technology Section.

2. Ultrasonic Machining (J. Krawczyk)

Holes were ultrasonically machined through ceramic rods for the NBS Instrumentation Applications Section.

3. SEM Technical Services (W. J. Keery)*

SEM photomicrographs of smoke particles were taken for the NBS Building Fires and Safety Section.

SEM photomicrographs of the metal surfaces at the connector-wire interface of an electrical outlet unit were taken for the NBS Materials and Composites Section.

4. Channel Electron Multipliers and Silicon Nuclear Radiation Detectors (Y. M. Liu)†

Evaluation of channel electron multipliers for the NASA Goddard Space Flight Center continued. Acceptance testing of four units for the AE-C and -D experiments and five units for sounding rocket auroral particles experiments was completed.

Measurement of dead layer thickness for three p-type surface-barrier detectors was carried out using the change in pulse height with charged-particle incident angle.

The pulse height and counting characteristics of a double-grooved lithium-drifted silicon detector were measured using a collimated proton beam.

5. Ribbon Wire Bonding (H. K. Kessler)+

Assistance to the Naval Electronics Laboratory Center, San Diego, in the implementation of NBS-developed ribbon wire technology on their pilot production continued. Bonds were made to gold thin film substrates received from NELC using

*NBS Cost Center 4254141

†NBS Cost Center 4254429

+NBS Cost Center 4254448

1.5 mil by 0.5 mil (38 μm by 13 μm) aluminum (1% silicon) wire. The average pull strength of the bonds showed much less variation from substrate to substrate than for those substrates initially received. Ribbon wire bonding tools made to NBS specifications for NELC were checked out and sent to NELC. Design changes to another series of round and ribbon wire bonding tools were completed and sent to the tool manufacturer. On these tools, the manufacturer will use the technique developed at NBS for polishing the wire feed hole (NBS Tech. Note 788, p. 35).

APPENDIX D
JOINT PROGRAM PUBLICATIONS

Prior Reports

A review of the early work leading to this Program is given in Bullis, W. M., Measurement methods for the Semiconductor Device Industry — A Review of NBS Activity, NBS Tech. Note 511, December, 1969.

Quarterly reports covering the period since July 1, 1968, have been issued under the title Methods of Measurement for Semiconductor Materials, Process Control, and Devices. These reports may be obtained from the Superintendent of Documents (Catalog) Number C.13.46:XXX) where XXX is the appropriate technical note number. Microfiche copies are available from the National Technical Information Service (NTIS), Springfield, Virginia 22151.

Quarter Ending	NBS Tech. Note	Date Issued	NTIS Accession No.
September 30, 1968	472	December, 1968	AD 681330
December 31, 1968	475	February, 1969	AD 683808
March 31, 1969	488	July, 1969	AD 692232
June 30, 1969	495	September, 1969	AD 695820
September 30k 1969	520	March, 1970	AD 702833
December 31, 1969	527	May, 1970	AD 710906
March 31, 1970	555	September, 1970	AD 718534
June 30, 1970	560	November, 1970	AD 719976
September 30, 1970	571	April, 1971	AD 723671
December 31, 1970	592	August, 1971	AD 728611
March 31, 1971	598	October, 1971	AD 732553
June 30, 1971	702	November, 1971	AD 734427
September 30, 1971	717	April, 1972	AD 740674
December 31, 1971	727	June, 1972	AD 744946
March 31, .1972	733	September, 1972	AD 748640
June 30, 1972	743	December, 1972	AD 753642
September 30, 1972	754	March, 1973	AD 757244
December 31, 1972	773	May, 1973	AD 762840
March 31, 1973	788	August, 1973	

Current Publications

As various phases of the work are completed, publications are prepared to summarize the results or to describe the work in greater detail. Copies of most such publications are available and can be obtained on request to the editor or the author.

Kessler, H. K., and Sher, A. H., Microelectronic Interconnection Bonding with Ribbon Wire, NBS Tech. Note 767 (April 1973).

Sawyer, D. E., Rogers, G. J., and Huntley, L. E., Measurement of Transit Time and Related Transistor Characteristics, AFWL Report TR-73-54 (9 March 1973).

Schafft, H. A., Failure Analysis of Wire Bonds, presented as part of a Workshop on Failure Analysis of Semiconductor Devices and Packages, 1973 Reliability Physics Symposium, Las Vegas, Nevada, April 4, 1973.

Sher, A. H., and Kessler, H. K., Microelectronic Interconnection Bonding with Ribbon Wire, presented at Third Annual Symposium on Hybrid Microelectronics, Baltimore, May 3, 1973.

Buehler, M. G., Thermally Stimulated Measurements: The Characterization of Defects in Silicon *p-n* Junctions, *Semiconductor Silicon/1973*, H. R. Huff and R. R. Burgess, eds., pp. 549-560 (Electrochemical Society, Princeton, New Jersey, 1973).

Leedy, K. O., Scanning Electron Microscope Examination of Wire Bonds from High-Reliability Microelectronic Devices, NBS Tech. Note 785 (July, 1973).

Harman, G. G., Ultrasonic Wire Bonding, presented at the 1973 International Hybrid Microelectronics Symposium, San Francisco, California, October 22, 1973.

Schafft, H. A., Methods for Testing Wire-Bond Electrical Connections, to be presented at the Third Symposium on Reliability in Electronics, Budapest, November 13-16, 1973; also published as NBS Tech. Note 786 (November, 1973).

Oettinger, F. F., and Gladhill, R. L., Thermal Response Measurements for Semiconductor Device Die Attachment Evaluation, to be presented at the 1973 International Electron Devices Meeting, Washington, D. C., December 3-5, 1973.

APPENDIX E
ANNOUNCEMENT OF SRM 1520, BORON-DOPED SILICON FOR RESISTIVITY MEASUREMENTS

The NBS Office of Standard Reference Material announces the availability of Standard Reference Material (SRM) 1520, Boron-Doped Silicon for Resistivity Measurements.

This SRM was developed in response to the request of ASTM Committee F-1 on Electronics. SRM 1520 is intended for use in calibrating the measurement of the resistivity of silicon wafers as measured by the four-probe method (ASTM Method F-84).

SRM 1520 consists of a pair of boron-doped silicon single-crystal wafers, one each with nominal resistivity 0.1 and 10 Ω·cm. The wafers have a <111> crystallographic orientation, and are approximately 4.2 cm in diameter and 1 mm thick. Measurements of dislocation density and oxygen content indicate both silicon crystals to be essentially dislocation free, and to have an oxygen density of less than 7×10^{17} and 1×10^{17} cm^{-3} for the 0.1 and 10 Ω·cm crystals, respectively.

The resistivity values of the individual wafers were measured using ASTM Method F-84. The single laboratory measurement, which included the effects caused by two operators and two instruments, yielded a 95 percent confidence interval for the average value of each wafer of less than ±1 percent. However, to make allowance for the as yet unknown variability between laboratories, which may be experienced in referee usage, the certified values for the individual wafers, based on the measurement procedure used in this study, are considered precise to ±2.5 percent of their stated values. A copy of ASTM Method F-84 which includes tables of geometry and temperature correction factors is provided with each set of wafers.

An interlaboratory test of the stability of the wafers over an extended period of time will be conducted. A report based on this test will be issued and the statement on the Certificate will be modified at that time if warranted.

Standard Reference Material 1520 may be ordered from the Office of Standard Reference Material, National Bureau of Standards, Washington, D. C. 20234. The price of each set is $425. Technical inquiries should be directed to J. R. Ehrstein, Room B-346, Technology Building, National Bureau of Standards, Washington, D. C. 20234.

APPENDIX F

STATUS OF MEASUREMENT TECHNOLOGY FOR CONTROL OF INTEGRATED CIRCUIT FABRICATION AND ASSEMBLY PROCESSES — A PRELIMINARY REVIEW

Beginning next quarter the scope of the Joint Program on Methods of Measurement for Semiconductor Materials, Process Control, and Devices will be expanded significantly with the inclusion of a new effort on Advancement of Reliability, Processing, and Automation for Integrated Circuits with the National Bureau of Standards (ARPA/IC/NBS), sponsored by the Defense Advanced Research Projects Agency (ARPA). This new effort, which addresses critical Defense Department problems in the yield and reliability of integrated circuits, responds to a need for improved measurement methods and associated technology for controlling and automating key processing and assembly procedures and is being developed in concert with the reliability laboratories of the three services. Its major thrusts are the development of well-documented test procedures and measurement technology for use on semiconductor device production lines and the dissemination of such information to the electronics community. Application of the output by industry is expected to contribute to higher yields, lower cost, higher reliability, and greater availability of special devices needed by the Department of Defense.

To assist in the selection of activities to be undertaken in this effort, initial consultations were completed with representatives of the electronics community to identify the more important measurement problems in process control for silicon wafer fabrication and device assembly primarily of bipolar and MOS digital integrated circuits. These consultations were made during visits to ten device manufacturing companies and one private research organization where discussions were conducted with a total of almost 100 technical people.

The generalized need expressed by many of the respondents was for more nondestructive, direct, and rapid production-type methods for measurement in order to reduce the appreciable number of silicon slices that would have to be sacrificed if all the necessary measurements were to be made, to avoid the need to infer product characteristics from tests on sample silicon slices, and to provide the faster feedback necessary to allow the desired degree of control on the production line.

The most critical measurement needs identified during the visits are ranked and reviewed briefly in the following paragraphs. The relative importance of the problem areas identified was gauged according to the number of organizations that mentioned the area as being important and the degree of interest or ranking that was indicated by the respondents.

Process control measurement problems of primary concern are with: (1) the starting silicon material in regard to defects and resistivity; (2) silicon diffused and epitaxial layers in regard to thickness, doping profiles, and sheet resistivity; (3) oxide films in regard to stability and impurities; (4) photolithographic and associated procedures in regard to mask inspection, photoresist materials and their use, and pin holes; and (5) hermeticity.

With regard to the starting silicon material and silicon layers there are a number of problem areas that were mentioned. There is a general need for improved methods for detecting and characterizing defects and contaminants, and for determining the effect they have on device yield and reliability. Among the defects mentioned were swirling patterns of vacancies, crystallographic defects, ion-implantation-induced defects, defects in epitaxial material, and back-lap defects.

Improvements in the measurement of resistivity of bulk silicon and diffused and epitaxial silicon layers and in the measurement of resistivity profiles of these layers was of general interest. A number of organizations expressed concern about resistivity inhomogeneities in silicon slices and the need for adequate methods for measuring them. Concerns were also expressed about the correction factors used with the spreading resistance method, about insufficient reproducibility of the four-probe method on a routine basis, and about the problems associated with the use of the four-probe method for measuring thin epitaxial layers. Those using the capacitance-voltage method for measuring profiles were generally not satisfied with the method.

Much concern was expressed in most of the organizations about the inadequacy of the methods for measuring junction depth and epitaxial film thickness. The concern is most acute for layers less than about 1 μm thick, which are now being more widely used. While many use the lap-and-stain method, no one expressed satisfaction with this method. Complaints about the need to interpolate between fringes and the difficulty of staining, especially for thin layers, were common. Problems mentioned with nondestructive methods employing infrared interferometry involved insufficient sensitivity and precision and inability to make quantitative measurements on epitaxial layers over buried layers because of out-diffusion, in addition to the inability to measure epitaxial layer thicknesses less than about 1 μm.

A strong need was expressed for improved means for characterizing oxides in MOS devices. Dissatisfaction with the capacitance-voltage method used to test for oxide stability was widespread. A typical comment was that the method could not be used to identify the reason for oxide instability. Some felt the method to be too slow and others felt it to be insufficiently sensitive to the level of impurities encountered that would have an effect on stability. Many felt that there should be a

standard method for judging oxide stability by specifying temperature-bias-time stress conditions and the allowed shift in threshold voltage as a result of these stresses. Fewer expressed a need to have adequate means of determining the kinds and levels of impurities that can lead to instability.

Great interest was expressed in the need for improved control of the photolithographic and associated procedures. There was a general and strong need to have a better means of inspecting photomasks. Present visual inspection methods are inadequate because of the time needed to make the inspection, the operator subjectivity, and the inability to detect all defects. The inability to detect random defects is of particular concern. It is felt that better inspection methods would significantly improve yield.

Great concern was expressed over the need to improve the methods for characterizing photoresist materials and photoresist films in use-type tests. Needs varied from knowing what characteristics to measure to how to measure these characteristics. Also, many were frustrated about the inadequacy of their methods for calibrating and determining the uniformity of the light used in photoresist exposure.

On the slice itself there is a desire to detect smaller pin holes (or defects) and potential pin holes, and to do this by non-destructive means if possible. Also, an often expressed need was one of being able to even define what a pin hole is.

Still another problem is the disagreement of the filar eyepiece and the double image shear methods for measuring oxide window dimensions and line width and separation on the mask and slice. Some suggested the need for length standards that could be used for calibration purposes to resolve the differences.

While control of the various assembly procedures is important to yield and reliability and processes such as die attachment and wire bonding continue to be of major importance, the problems with hermeticity testing appear to be particularly frustrating to many in the industry. Common complaints are: the lack of agreement between the helium leak detector and the radioisotope methods and the problems that ensue at the vendor-user interface; the lack of adequate leak-rate standards; and the subjectivity of the bubble test for detecting large leaks.

There are a number of other problem areas of somewhat less relative importance by virtue of the smaller number of times they were mentioned. These process control measurement problems are in the control of incoming materials, ion implantation processes, and surface cleanliness.

With regard to incoming materials there is a need for fast, production-line methods to test for impurities in acids, solvents, dopants, etc. In general, there

is the additional problem of not knowing which kinds of impurities and at what concentrations they may have a potentially harmful effect on device yield and reliability. Maintenance of piece-part quality is also a common problem.

Of the organizations involved in the use of ion implantation, there is the commonly expressed need to improve methods for monitoring and controlling the number and uniformity of the ions implanted.

Finally, there is no satisfactory method for the production line that can determine if selective localized areas on the device slice are sufficiently clean and free of residues for metallization deposition or for wire bonding.

The following measurement areas were also mentioned: temperature in epitaxial reactors and diffusion furnaces; gas flow rates; metallization and oxide thickness; phosphorus concentration in glass overcoats; dielectric breakdown characteristics of oxides; characteristics of silicon nitride layers; wafer warpage; metallization step coverage; and test pattern usage. (H. A. Schafft)

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4251126, 4252128, 4254115, 4251140, 4254140, 4254425, 4259522, 4250555, 4259533, 9252535.

16. ABSTRACT (A 200-word or less factual summary of most significant information. If document includes a significant bibliography or literature survey, mention it here.)

This quarterly progress report, twentieth of a series, describes NBS activities directed toward the development of methods of measurement for semiconductor materials, process control, and devices. Significant accomplishments during this reporting period include (1) completion of an initial identification of the more important problems in process control for integrated circuit fabrication and assembly as a basis for an expanded effort to be conducted in cooperation with ARPA, (2) completion of preparations for making silicon bulk resistivity wafer standards available to the industry, and (3) undertaking of new work to establish the relationship between carrier mobility and impurity density in silicon and to investigate test patterns for use in process control and evaluation. Because of the general applicability of the first of these, a summary of the findings is presented in a separate appendix. Work is continuing on measurement of resistivity of semiconductor crystals; characterization of generation-recombination-trapping centers, including gold, in silicon; evaluation of wire bonds and die attachment; study of scanning electron microscopy for wafer inspection and test; measurement of thermal properties of semiconductor devices; determination of S-parameters and delay time in junction devices; and characterization of noise and conversion loss of microwave detector diodes. Supplementary data concerning staff, standards committee activities, technical services, and publications are also included as appendices. This is the last report in this form; future reports in this series will appear under the title, Semiconductor Measurement Technology.

17. KEY WORDS (Alphabetical order, separated by semicolons)

Beam leads; carrier lifetime; delay time; die attachment; electrical properties; electronics; epitaxial silicon; generation centers; gold-doped silicon; methods of measurement; microelectronics; microwave diodes; mobility; pull test; recombination centers; resistivity; resistivity standards; scanning electron microscopy; semiconductor devices; semiconductor materials; semiconductor process control; silicon; S-parameters; spreading resistance; thermal resistance; thermally stimulated properties; trapping centers; wire bonds.

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